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Engineering Support for High Power Density Gallium Nitride Microwave Transistors

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14. ABSTRACT

Continuous and pulsed RF and IV on-wafer characterization was performed on gallium nitride high electron mobility transistors supplied by three independent sources. Measurements were performed over a range of temperatures and bias conditions to permit an indepth understanding of self-heating effects. Analysis was also performed to investigate substrate effects.

15. SUBJECT TERMS

Microwave power FETs, GaN HEMTs, Self-heating effects, Pulsed load-pull

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Thanks are also extended to the engineers at Maury Microwave for assistance with load-pull equipment.

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1. Executive Summary

Georgia Tech completely characterized gallium nitride (GaN) devices from three separate suppliers and validated that GaN devices, at X-band, can produce over five times the power density of state of the art GaAs/InP-based FETs and HBTs. These results are based on early GaN high electron mobility transistors and even higher performance has been demonstrated. We investigated trapping effects, substrate effects and thermal issues and provided "value added" feedback to the DoD sponsored GaN device suppliers. Georgia Tech also wrote and published six papers based on this work. This measurement program demonstrates that GaN device technology is maturing and revolutionary performance is possible; however, significant materials and process details must be refined to produce the stable device characteristics that are essential for the development of GaN-based monolithic microwave integrated circuits (MMICs)

This report summarizes the characterization of gallium nitride (GaN) transistors supplied to Georgia Tech by Cree, Inc., Cornell University and Cree Lighting, a division of Cree, Inc. Cree, Inc. supplied a total of twenty devices having gate widths of 0.25 and 1.5mm respectively. These devices were mounted on a copper heat spreader. Cornell provided eight devices on a copper carrier. Cree Lighting provided one-fourth of a two-inch diameter wafer that was partially through front side processing. Devices, that did not have air bridges, were available for characterization.

This work was performed at the Georgia Tech Research Institute (GTRI) in an advanced microwave measurements laboratory equipped by a joint effort between GTRI and the School of Electrical and Computer Engineering (ECE).

GaN-based transistors operate at drain voltages of 30 to 50 volts or more compared to nominally 10 volts for gallium arsenide-based devices. As a result, test equipment designed for GaAs devices was not suitable in all cases for GaN device characterization. GTRI/ECE designed special test setups and procured equipment required to perform both small and large signal analysis. Drain bias supplies and a high power, traveling wave tube amplifier, for input signal amplification, were unique pieces of equipment that were added to permit characterization of the GaN devices.

GTRI met with Cree personnel at their facility in Durham, NC to discuss measurement support for GaN microwave power transistors. Cree was very receptive and open to discussions with GTRI and provided helpful suggestions regarding load pull measurements and equipment to measure high power devices. GTRI acquired additional high power test equipment based on Cree's recommendations that included Maury Microwave Load Tuners and Giga-tronics Dual Channel Power Meter and two Peak Power Sensors. Dr. Richard Shealy, presented a seminar at Georgia Tech and personally delivered the Cornell devices.

GTRI/ECE performed an extensive sequence of characterization tests. Direct current (DC) tests permitted investigation of trapping effects. Evidence of trapping appears as a kink in DC-IV curves. We studied the appearance/disappearance of trapping effects using delay between each V_{ds} sweep and by adjusting the V_{ds} boundaries. Pulsed IV tests were performed to investigate device performance in the absence of self-heating. Continuous and pulsed RF and IV on-wafer characterizations were performed at different temperatures on power GaN HEMTs. At high drain voltage (above 20 V) if there is no delay in between drain sweep, a kink appears in I_{DS}-V_{DS} characteristics. This is interpreted as a trap effect that is only activated when the drain bias is high enough.

S-parameter tests were performed to obtain the small signal characteristics of the devices. Cryogenic measurements at 65K using both DC and pulse IV demonstrated the absence of self-heating effects at low temperature. Large signal analysis of GaN transistors, using pulsed load pull, was the main thrust of this program.

Devices, from each source, demonstrated power densities from three to five times higher than state of the art GaAs-based pesudomorphic high electron mobility transistors. Power added-efficiencies were on the order of 25-40 percent. These device results are encouraging: however, there are stability issues in GaN devices that must be solved. GTRI assesses that these instabilities may be due in part to the surface states and high field regions. Advanced surface passivation and gate recess processes may help eliminate the instabilities.

2. Introduction

Solid-state amplifiers are replacing traveling-wave-tube-amplifiers (TWTAs) for microwave power applications. However, the low operating voltages of solid-state devices lead to a large device periphery resulting in high device and circuit complexity, reducing production yield and reliability. Wide-bandgap technologies like GaN can achieve power densities of over five times higher than conventional GaAs/InP-based high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). Use of these wide bandgap devices and circuits will ultimately result in reduced circuit complexity, improved gain-bandwidth product and potentially lower cost as the technology reaches maturity. Numerous military (e.g. radar) and commercial applications (e.g. communication systems) will benefit from the development of this technology.

In order to provide a mature technology based on GaN, it is crucial to fully investigate wide bandgap electronic devices and circuits. This includes the understanding of the device technology, its reliability, and the development of circuits and system applications. A key aspect in maturing this technology is complete electrical characterization as a function of frequency, bias conditions and temperature. This characterization serves as the basis for accurate high power microwave circuit models that permit development of monolithic microwave integrated circuits (MMICs) that form the building blocks for larger systems.

GTRI/ECE has developed a world-class microwave characterization facility and used this facility and some enhancements to characterize GaN HEMTs supplied by Cree, Inc., Cornell University and Cree Lighting who fabricated devices on related DOD-sponsored programs.

The following sections present details equipment modifications required to support the GaN device measurements, characterization systems used in the analysis, device characterization and investigation of self-heating effects, substrate effects and thermal analysis. Copies of our published papers are included in the appendix.

3. Characterization Systems

3.1 DC IV

A first step to characterize devices is to perform DC-IV measurements. Figure 1 presents a schematic of the DC setup used. The DC-IV setup includes a PC connected to HP 4145 and HP 4142 Semiconductors Parameter Analyzers through a HP interface buss (HIPB). This setup permits measurement of basic parameters such as knee voltage, saturation current, transconductance and breakdown voltage. Self-heating effects, discussed a subsequent section and can also be investigate with this setup.

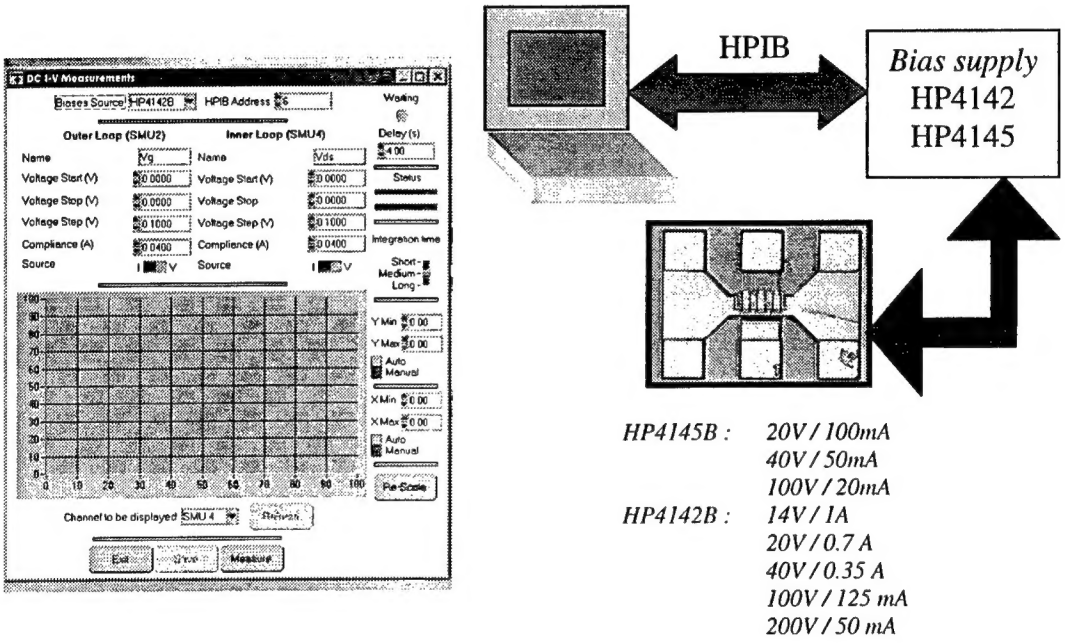


Figure 1. Schematic of a DC-IV System.

3.2 Pulsed IV

Figure 2 presents a schematic of our pulsed-IV system. Two pulse generators from the Agilent 8110 series are used for bias purposes. Drain current is monitored with a digitizing scope through an AM503B current amplifier from Tektronix. Both drain and gate voltages are monitored with the same scope using its high internal impedance capability.

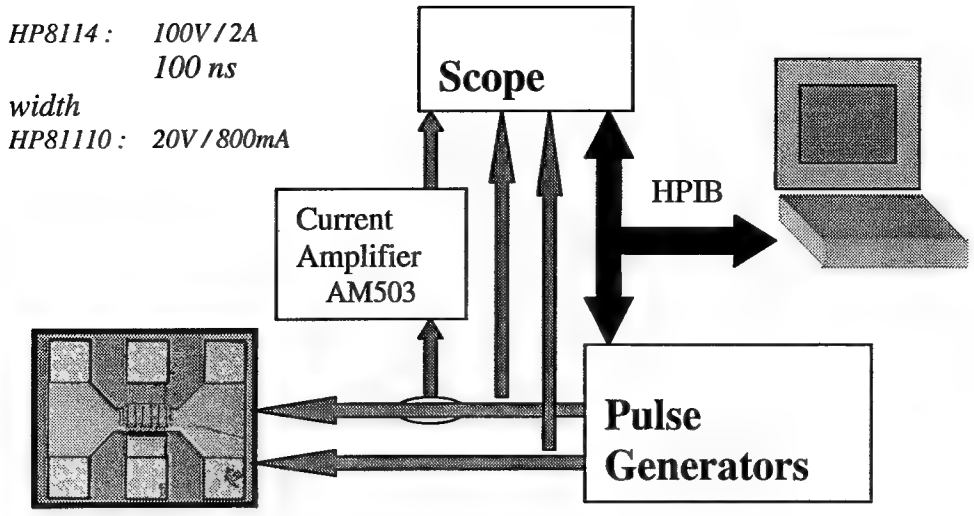


Figure 2. Schematic of the Pulsed-IV System.

Figure 3 shows the I_{DS}/V_{DS} characteristics at various V_{GS} of a 2-finger device (gate width is 250 μm) under pulsed and continuous conditions. During the measurement, both gate and drain side were pulsed. The signal period was fixed at 15 μs, the pulse width on the gate side was 1.5 μs, and 1 μs on the drain side. The pulse on the drain side was delayed by 200 ns from the gate pulse. **We observe that under pulsed conditions there is no decrease in drain current when increasing the drain bias.**

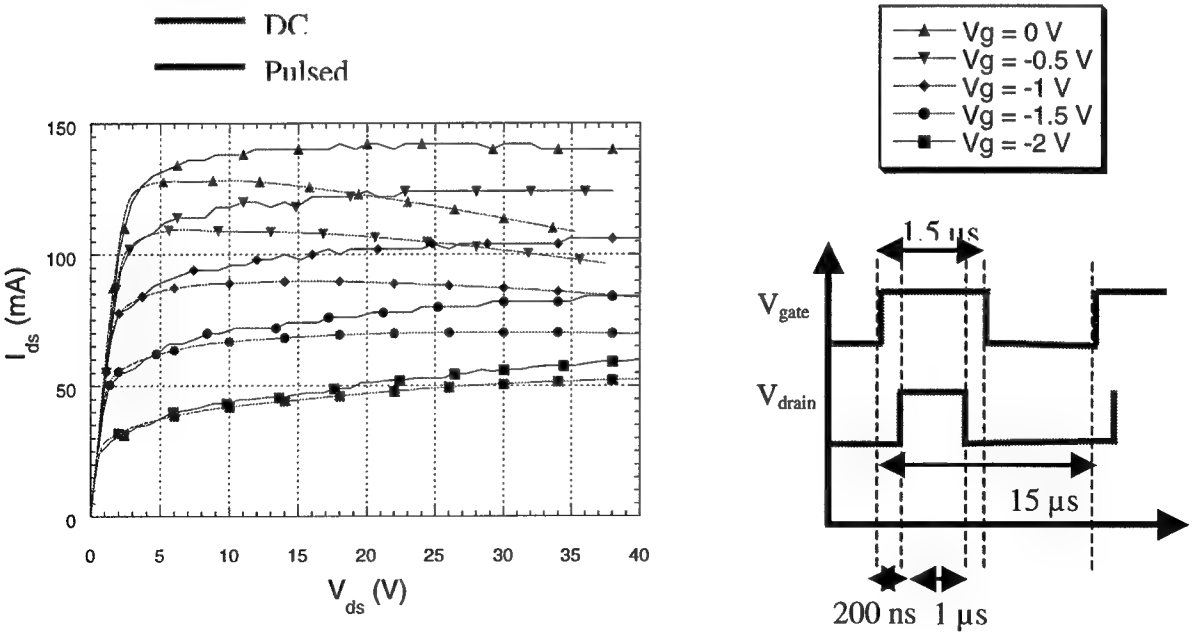


Figure 3. Difference Between DC-IV and Pulsed-IV Characteristics at Room Temperature.

3.3 Cryogenic Probing System

On-wafer measurements have been carried out at temperatures as low as 65K using a custom made cryogenic probe station. The cryogenic probing system, shown in Figure 4 and Figure 5, contains ports for RF and DC cables, temperature sensors, vacuum pumps, coplanar wave-guide probes with manipulators, and a closed-cycle helium refrigerator cold head. The device under test (DUT) is mounted on the cold wafer stage and the test chamber is evacuated to prevent frost build up and large thermal grading when cooling the chamber. A thermocouple mounted in the cold head wafer stage is used to measure the temperature and all of our temperature data are based on measurement at this point. Probe positioning is accomplished with the manipulators by observing the device through the view port with a microscope as shown in Figure 6.

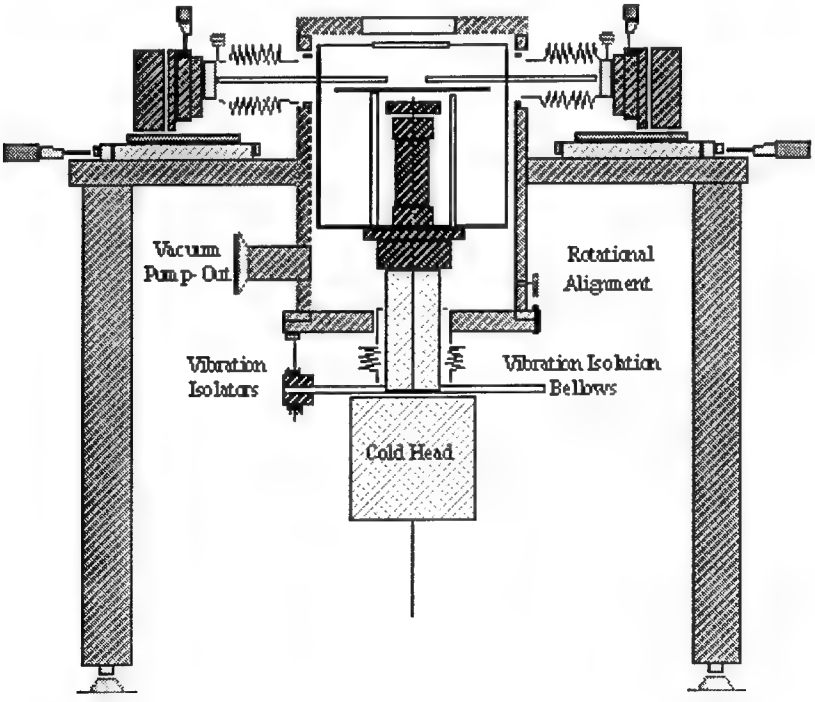


Figure 4. Side View of Cryogenic Measurement Chamber.

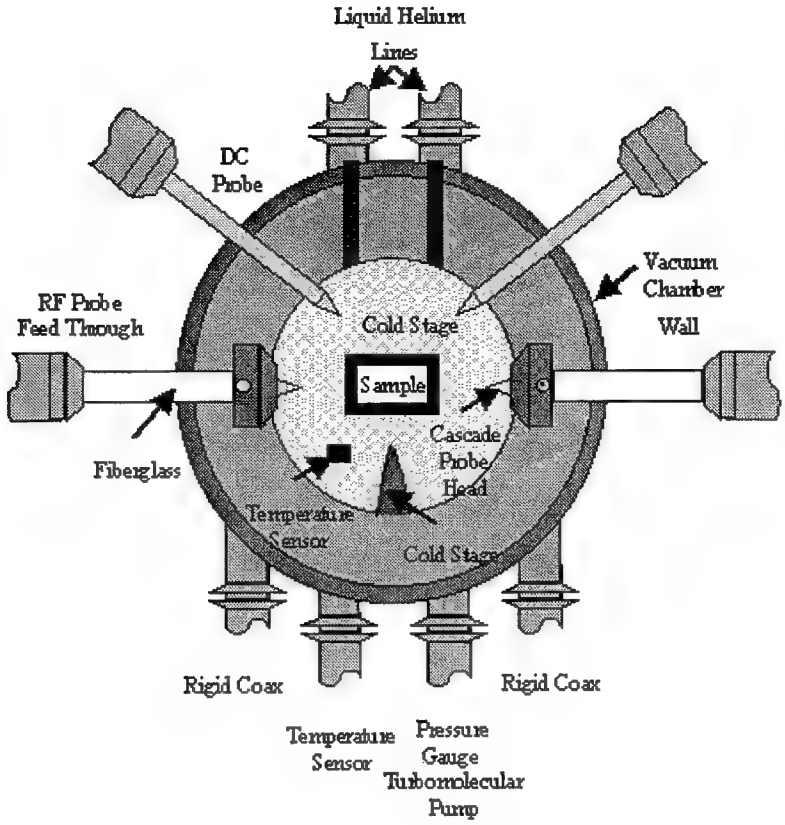


Figure 5. Top View of Cryogenic Measurement Chamber.

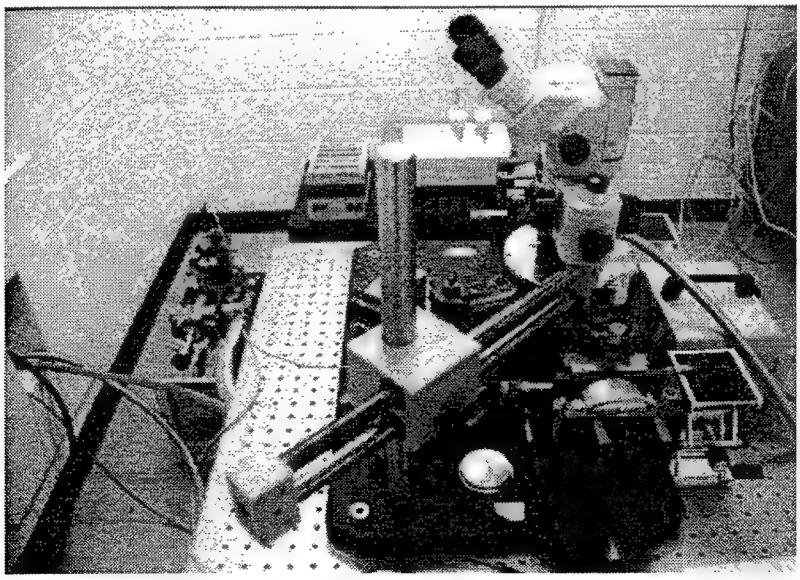


Figure 6. Viewing port of the Cryogenic System with Microscope Installed.

3.4 Small Signal Characterization

The system used to characterize the devices under small-signal conditions is based on an HP8510C.Network Analyzer System that includes an S-parameter test set and a synthesized signal source. All tests are performed under HPIB control as shown in the diagram in Figure 7.

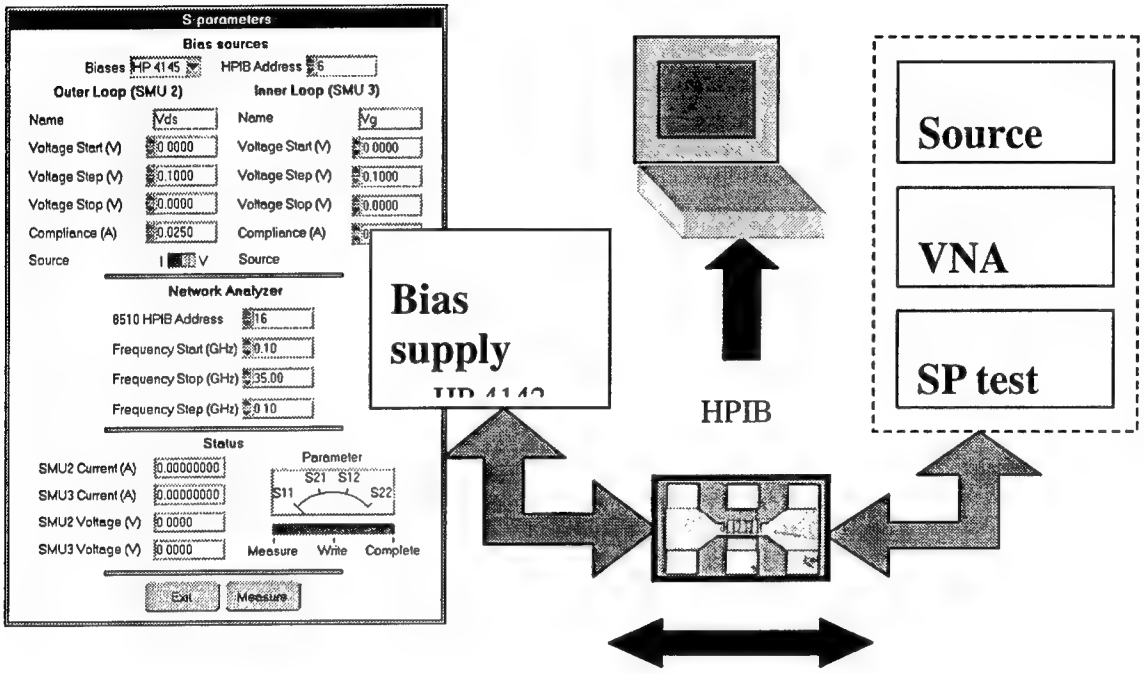


Figure 7. Schematic of the Small-signal Characterization System.

3.5 CW/Pulsed Load-Pull

Figure 8 is a block diagram of the CW/pulsed load pull system. The system includes Maury Microwave load tuners, a Giga-tronics dual channel power meter and two Giga-tronics peak power sensors. The tuners can handle up to 50W in CW mode and can operate from 1.8 to 18 GHz after adequate calibration. A 10W traveling wave tube amplifier (TWTA) is available for measurements between 8-12 GHz.

An S-parameter calibration, of all elements (fixtures, bias tees, couplers, cables, adapters…) inserted after the source tuner, is used to retrieve the actual power at the input and output of the DUT. **To our knowledge we are the first to measure the reflected power under pulsed conditions allowing us to extract the power gain (G_P) of the DUT in addition to the transducer gain (G_T).** Figure 9 is a photograph of the CW/pulsed load pull system and Figure 10 shows the wafer probe region with SiC substrate in place.

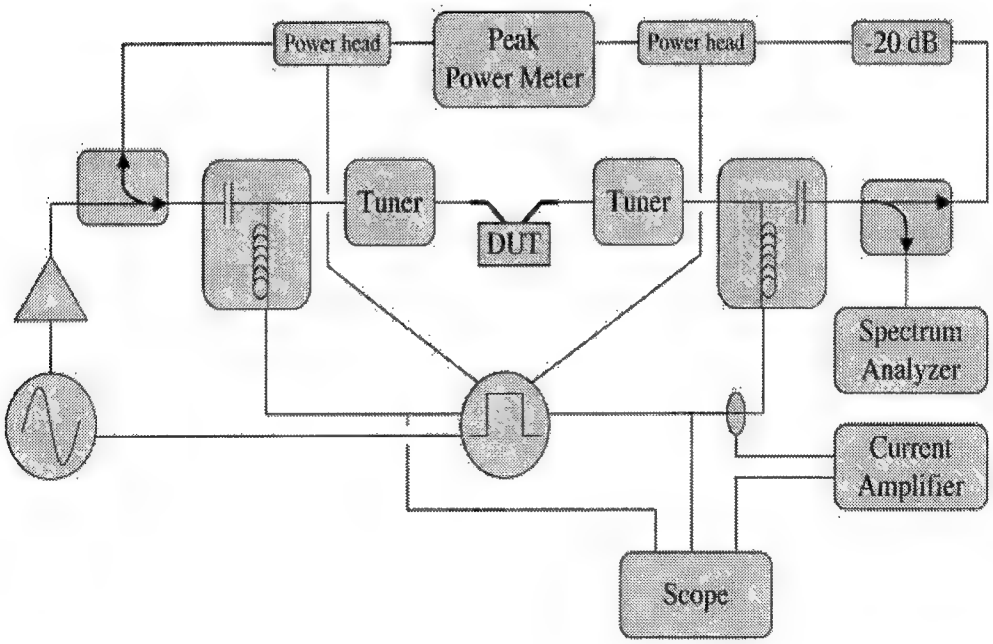


Figure 8. Diagram of the CW/Pulsed Load Pull Test Setup.

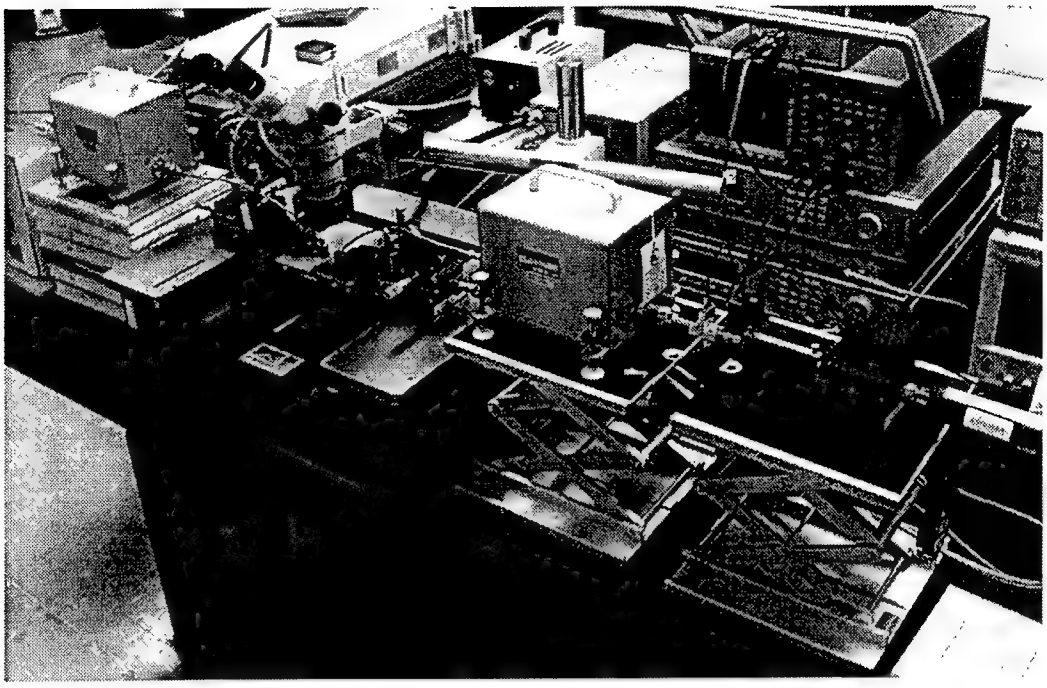


Figure 9. Photograph of the CW/Pulsed Load Pull Test Setup.

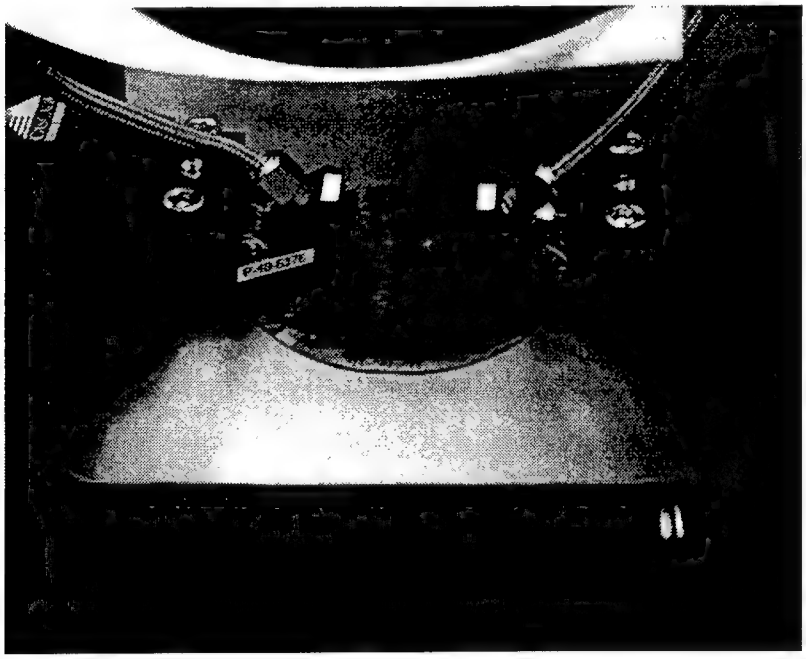


Figure 10. Wafer Probe Region of the CW/Pulsed Load Pull System.

4. Device Characterization

4.1 Cree (Durham)

GTRI met with Cree personnel at their facility in Durham, NC to discuss measurement support for GaN microwave power transistors. Cree was very receptive and open to discussions with GTRI and provided helpful suggestions regarding load pull measurements and equipment to measure high power devices. Cree personnel included:

John Palmour	Director of Advanced Devices
Jim Milligan	Manager, Microwave Military Programs
Scott Allen	Manager, RF Engineering
Scott Sheppard	Device Scientist
Bill Pribble	MMIC Design Engineer

Cree provided plots of their basic device structures shown in Figure 11 and Figure 12. Figure 11 is a layout drawing of the smallest test device consisting of two parallel fingers each 125 microns long resulting in a gate periphery of 0.25 mm. Figure 12 shows a 1.5 mm device layout. Both devices require on-wafer probes having a pitch of 250 microns. The 0.25mm device can be probed immediately after gate formation since air bridges and backside vias are not required.

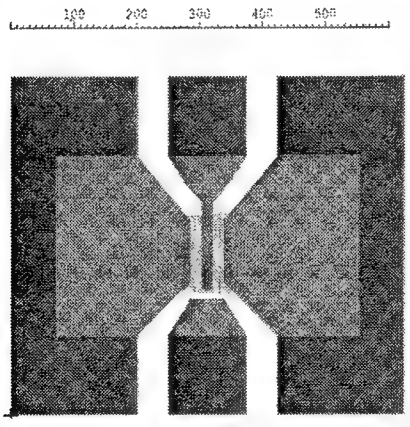


Figure 11. Cree's "Gate FET' Layout with Two Parallel Fingers and Shared Drain.

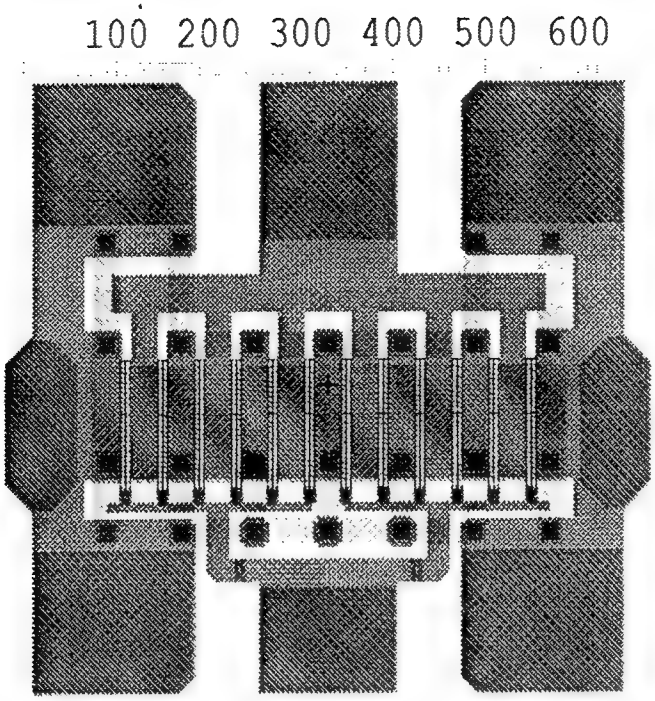


Figure 12. Twelve Finger, Air Bridged GaN Transistor having 1.5mm of Gate Periphery.

Cree recommended that GTRI start with the 0.25mm device and perform room temperature IV, S-parameter and load pull characterization. Room temperature cw load pull measurements were correlated with Cree's results prior to performing pulsed load pull or load pull as a function of temperature. Cree was particularly interested in how GTRI mounts GaN chips for testing. Figure 13 is a diagram of the scheme that we currently use. A 15-mil beryllium oxide (BeO) substrate having a thermal conductivity of 3W/cm-K is used. Cree suggested that we consider a SiC wafer having a thermal conductivity of 4-5W/cm-K. GTRI has the ability to eutectically solder the chips to metallized substrates. GTRI has experience in the use of type IIa diamond heatsinks for thermal spreading on IMPATT diode power combiners. Type IIa diamond has a thermal conductivity of approximately 20 W/cm-K. Cree recommended that GTRI also consider adding IR imaging to measure channel temperatures.

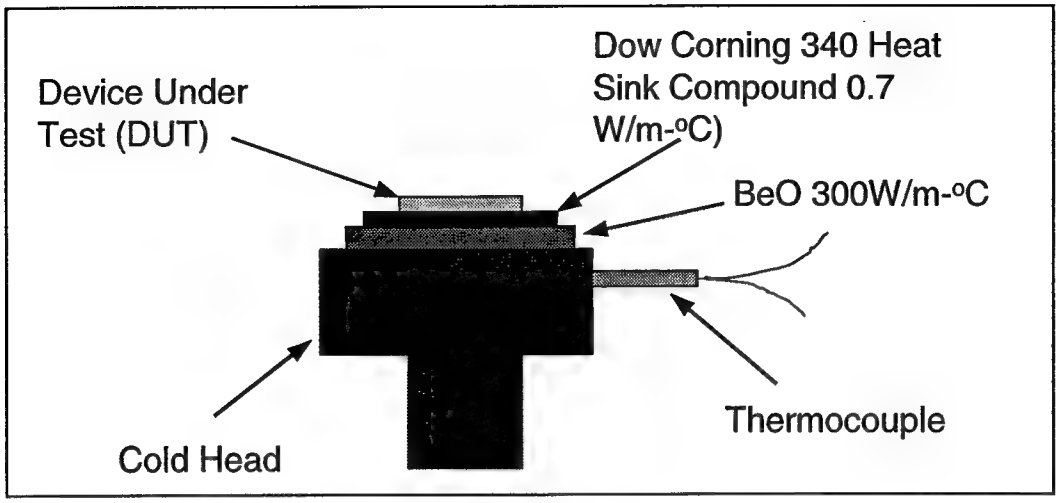


Figure 13. Device Mounting Scheme for GTRI's Cryogenic Measurement System.

GTRI and Cree discussed the requirements to make isothermal load pull measurements. **Cree indicated that the pulse width should be less than a few microseconds for on-wafer measurements.** This is consistent with information provided by Hewlett Packard in a presentation at the 1996 Device Test Seminar titled " Measurement Solutions for Testing Base-Station Amplifiers. Cree stated that GTRI would need to provide at least 25 dBm of power at the input of the device under certain input match conditions. Cree also indicated that GTRI could expect a device gain in the range of 10-15 dB. Pulsed load pull was discussed in detail. Scott Allen indicated that GTRI could expect much different results if we pulse the gate bias as opposed to the drain bias. Bill Pribble suggested using a bias pulse of not more than 10 microseconds and an RF pulse of 5 microseconds centered in the bias pulse.

Other tests that could be helpful in investigating performance limitations due to heating versus defects, include pulsed RF vs temperature, investigation of waveforms at lower frequency, transconductance dispersion, peak drain current vs temperature and power density vs temperature.

GTRI acquired additional high power test equipment based on Cree's recommendations that included Maury Microwave Load Tuners and Giga-tronics Dual Channel Power Meter and two Peak Power Sensors. An accurate pulsed load-pull system capable of measuring the reflected power has been built and utilized to measure RF power characteristics of GaN HEMTs at

different temperatures. Additionally an improved small-signal model for power GaN HEMT that incorporates the geometry of the device has been developed for various temperatures.

Cree, Inc provided 12 GaN HEMTs in three different types on a common copper carrier. Figure 14 shows photographs of the three device types. Gate width per finger is fixed at 125 μm and the gate length is 0.3 μm.

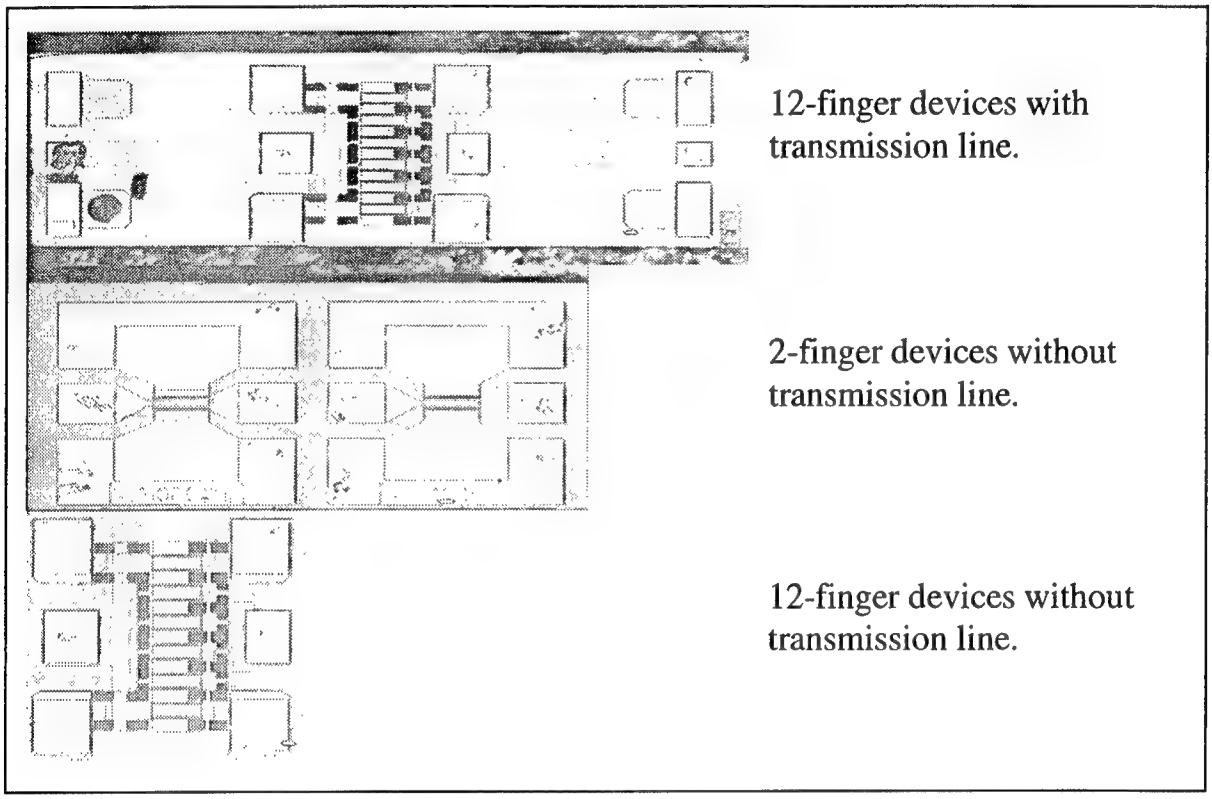


Figure 14. Photographs of GaN HEMTs from Cree, Inc.

Continuous and pulsed RF and IV on-wafer characterizations were performed at different temperatures on power GaN HEMTs. At high drain voltage (above 20 V), if there is no delay in between drain sweep, a kink appears in $I_{DS}(V_{DS})$ characteristics. This is interpreted as a trapping effect that is only activated when the drain bias is high enough.

Pulsed IV measurements showed that at temperatures less than 150K the drain current is saturated for all available pulse widths. This implies that there are no heating effects on the DC characteristics below 150K for these devices in this mounting scheme.

Pulsed RF measurements were made at 10GHz with a 3.4μs pulse width on the gate, a 3.2μs pulse width for the drain, and a 3μs pulse width for the RF signal. Measurements were

made at various lattice temperatures. **The power gain, measured under continuous and pulsed mode remains similar, however the drain current is observed to be less important under pulsed condition when the RF power at the input of the DUT is less than 16dBm, suggesting an improvement of the power added efficiency under pulse condition of operation at low RF power. Reducing the temperature of operation down to 100K enhances the power gain of the device and the drain current is reduced when the applied RF power at the input of the device does not exceed 13dBm.**

On-wafer measurements were carried out at temperatures as low as 65K using the custom made cryogenic probe station described earlier in Section 3. Figure 15 illustrates $I_{DS\ as}$ a function of V_{DS} for various V_{GS} of a 2-finger device. Figure 15 (a) presents results for drain voltages up to 10V. Figure 15 (b) shows measurements for drain bias up to 40V. **It is important to note that Figure 15 (a) is not a zoom of Figure 15 (b) but comes from a separate measurement.** Both Figures present results with delay (red curves) and without delay (blue curves) between each drain sweep. The delay was fixed at 60 seconds. As we can see, when the drain voltage reaches high values (above 20 V), if there is no delay in between drain sweep, a kink appears in $I_{DS}(V_{DS})$ characteristics. This is interpreted as trap effect. Those traps seem to be activated when the drain bias is high enough.

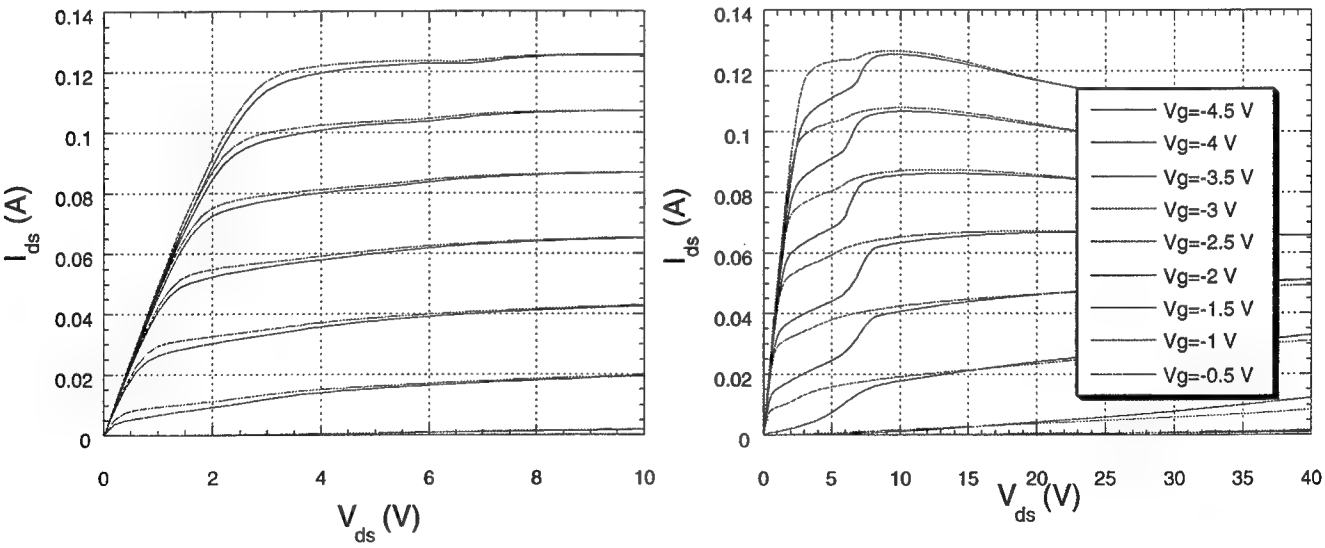


Figure 15. (a) Two Finger Device at 10V. **(b) Two finger Device at 40V.**

Figure 16 illustrates typical DC-IV results of a 12-fingers device (gate width = 1500 μm). A delay of 60 seconds has been applied between each drain voltage sweep to get rid of trap effect. Figure 16 (a) presents I_{DS} (V_{DS}) characteristics for various V_{GS}. Figure 16 (b) shows I_{GS} (V_{DS}) characteristics for various V_{GS}. The gate bias has been swept from –4.7 Volts to –1.4 Volts. These measurements have been performed at room temperature. It is noteworthy that in Figure 16 (a) when V_{GS} is greater than –2 Volts, I_{DS} (V_{DS}) curves exhibit a negative slope above a certain drain bias. This is an evidence of self-heating effect of the device.

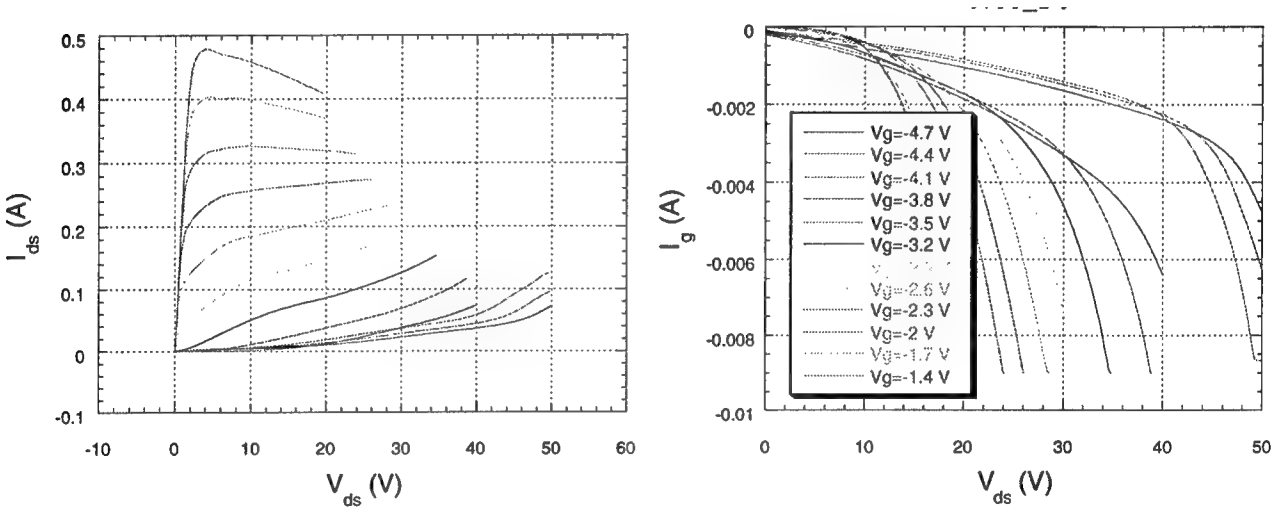


Figure 16. (a) I_{DS} Versus V_{DS} on a 1.5mm Device. (b) I_G Versus V_{DS}.

Figure 17 shows $I_{DS}(V_{DS})$ characteristics at various V_{GS} of a 2-finger device (gate width = 250 μm) under pulsed and continuous conditions. During the measurement both gate and drain side were pulsed. The signal period was fixed at 15μs, the pulse width on the gate side was 1.5μs, and 1μs on the drain side. The pulse on the drain side was delayed by 200 ns from the gate pulse. **Under pulsed conditions, there is no decrease of drain current when increasing the drain bias.** Figure 18 shows the same kind of measurement as Figure 17 but at a temperature of 65 K comparing $I_{DS}(V_{DS})$ at various V_{GS} under pulsed and continuous conditions. At 65K, CW and pulsed characteristics are almost identical and there is no negative slope in the characteristics. This is interpreted as an absence of self-heating effect throughout the entire drain voltage range used.

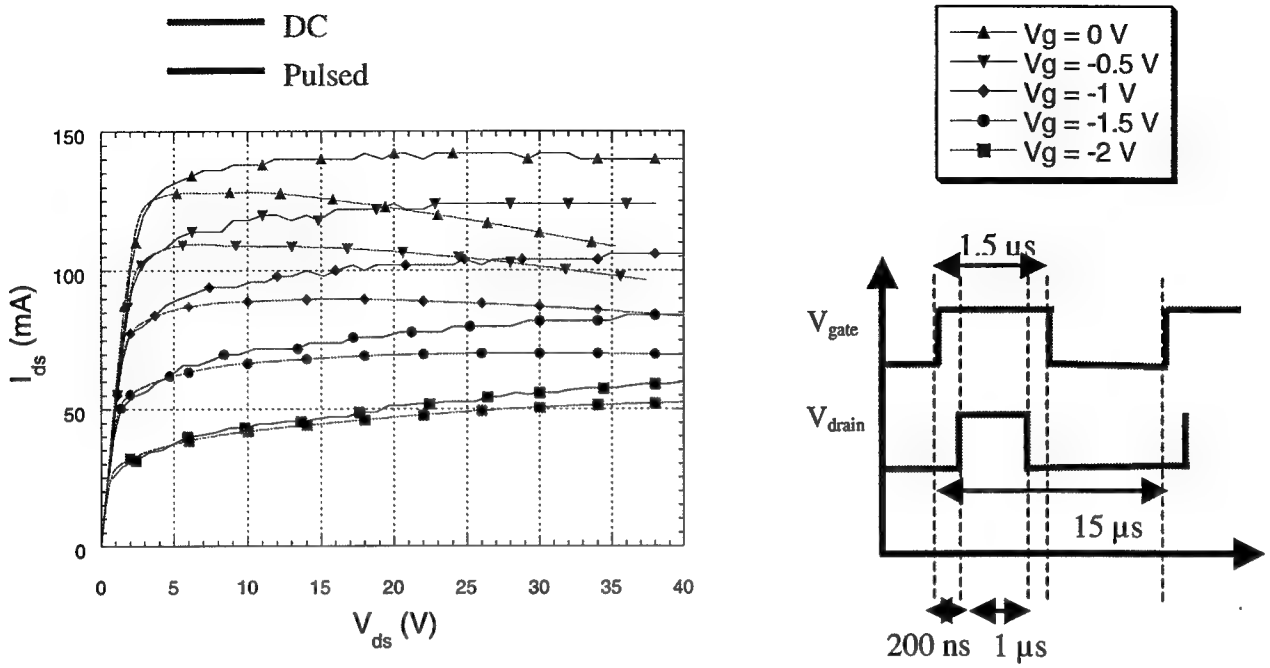


Figure 17. Comparison between DC-IV and Pulsed-IV Characteristics at Room Temperature.

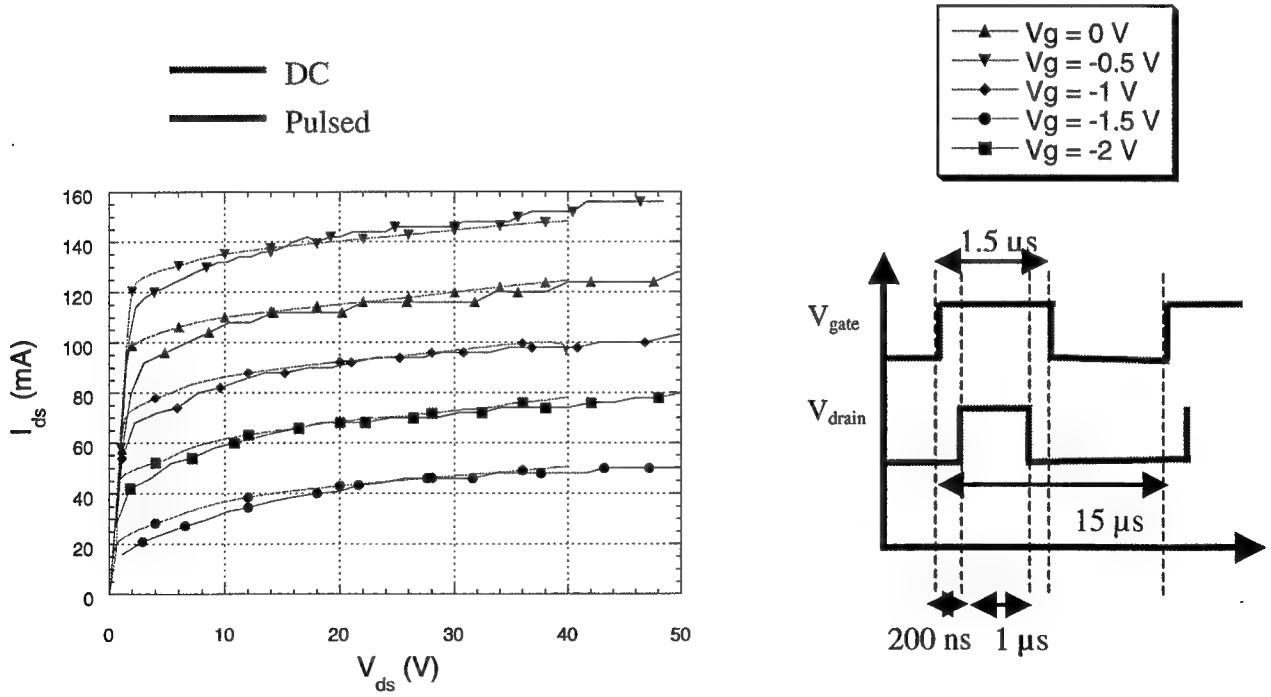


Figure 18. Comparison between DC-IV and Pulsed-IV characteristics at T = 65 K.

Figure 19 shows the effect of gate duty cycle on the drain current characteristics $I_{DS}(V_{DS})$ at $V_{GS} = 0$ Volts. The signal period is fixed at 150 µs and the gate duty-cycle is swept from 1% to 100% (continuous bias). The drain pulse is a little shorter to allow a centering with the gate pulse. We observe that by gradually reducing the duty-cycle the slope of $I_{DS}(V_{DS})$ increases and stops being negative. This is interpreted as a gradual switch into a heat free environment.

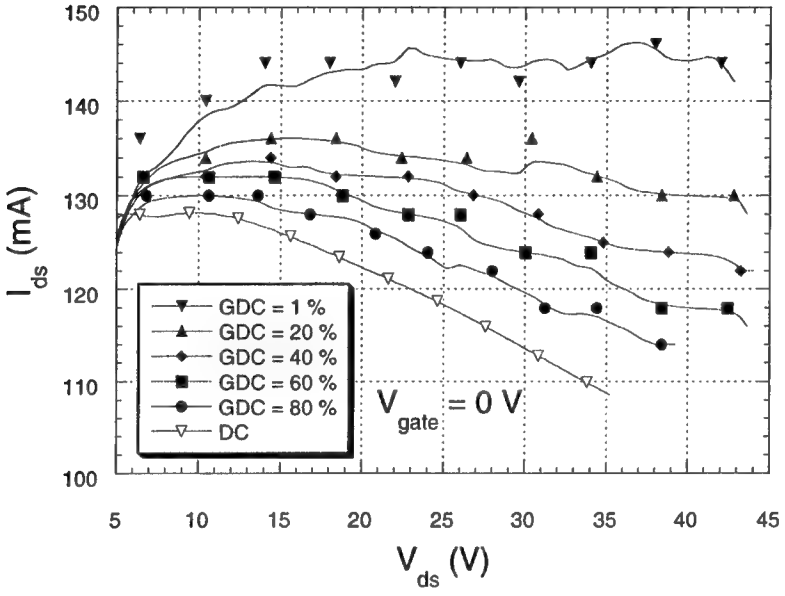


Figure 19. Influence of Duty-cycle on Drain Current.

It is possible to switch to a heat free regime, by reducing the pulse width even at fixed bias conditions and temperature. We define the pulse width threshold as the maximum pulse width to achieve such isothermal environment. The method to evaluate this threshold is to monitor the drain current at fixed bias and temperature and to sweep the pulse width. Saturation of drain current means that the current pulse width is below the pulse width threshold. Figure 20 shows the results obtained on a 2-finger device at $V_{DS} = 45$ V, and $V_{GS} = 0$ V, for various external temperatures, and with a signal period of 100 µs. From these curves, it is possible to evaluate a pulse width threshold (at these bias conditions and temperature). Below 150 K, the drain current saturates for all pulse widths, meaning that there is no heating effect even for nearly DC conditions. Above 250 K, the drain current did not saturate for a pulse width as low as 1 µs. For temperatures in between, it was possible to determine a pulse width threshold.

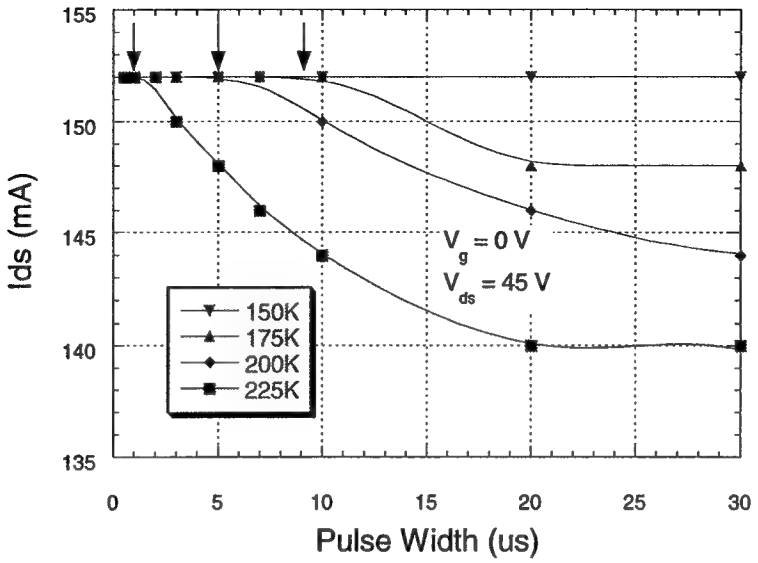


Figure 20. Determination of Pulse Width Threshold for Various Temperatures.

Figure 21 presents a plot of these pulse width thresholds versus temperature for 2 different bias conditions. We observe that at lower bias conditions it is possible to achieve a heat free environment at higher temperature at similar duty-cycle.

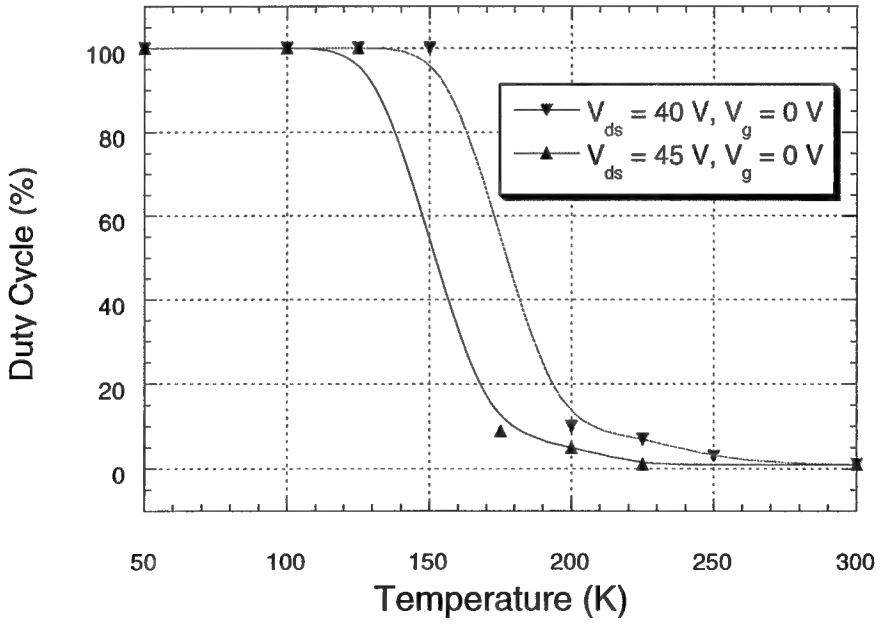


Figure 21. Pulse Width Threshold Versus Temperature at Various Bias Conditions.

Figure 22 shows $I_{DS}(V_{DS})$ at V_{GS} = 0 V, for various duty-cycle of drain and gate. The curves illustrate the device response if both drain and gate are pulsed at low duty-cycle, if only the drain is pulsed at low duty cycle, and also if both drain and gate are pulsed at high duty cycle. Pulsing only the drain at low duty cycle, and pulsing both gate and drain at low duty-cycle give similar results. This measurement has been performed on a 2-fingers device (gate width = 250 μm) with a signal period of 15 μs. GDC means Gate Duty Cycle, and DDC means Drain Duty Cycle.

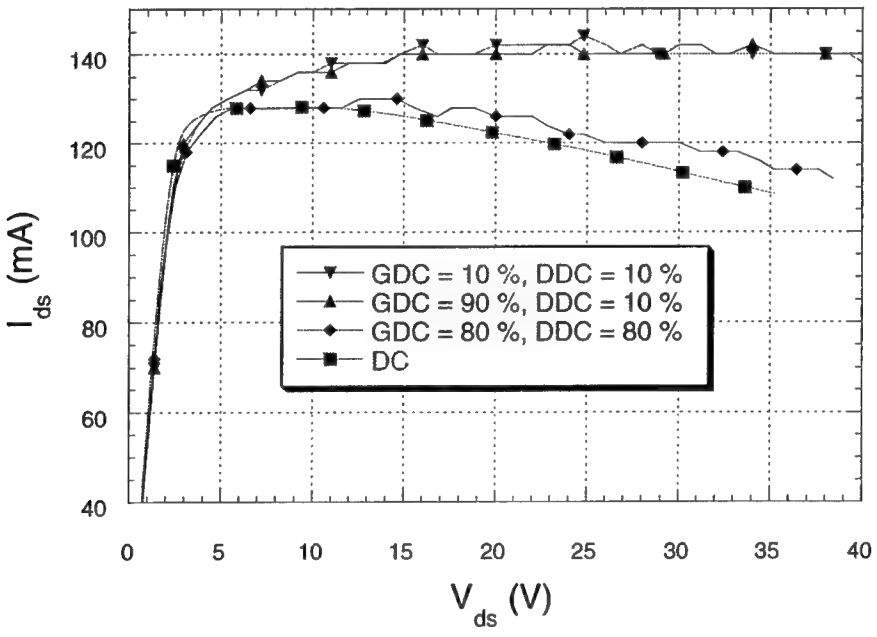


Figure 22. Comparison between Pulsing both Gate and Drain, and only the Drain.

Small-signal measurements were performed at various temperature and bias conditions on 2-fingers and 12-fingers devices. Calculation of short circuit current gain (h_{21}), and calculation of maximum available gain ($G_{A,\,Max}$) have been performed from S-parameters measurements, in order to extract the cutoff frequency as well as the maximum frequency of oscillation. Figure 23shows h_{21} and $G_{A,\,Max}$ versus frequency at various temperatures, and at fixed

bias condition. **The cutoff frequency f_T increases from 24 GHz to 26 GHz when reducing the temperature from 300 K down to 150 K, and the maximum frequency of oscillation f_{Max} goes from 27 GHz to 32 GHz when reducing the temperature from 300 K down to 150 K.**

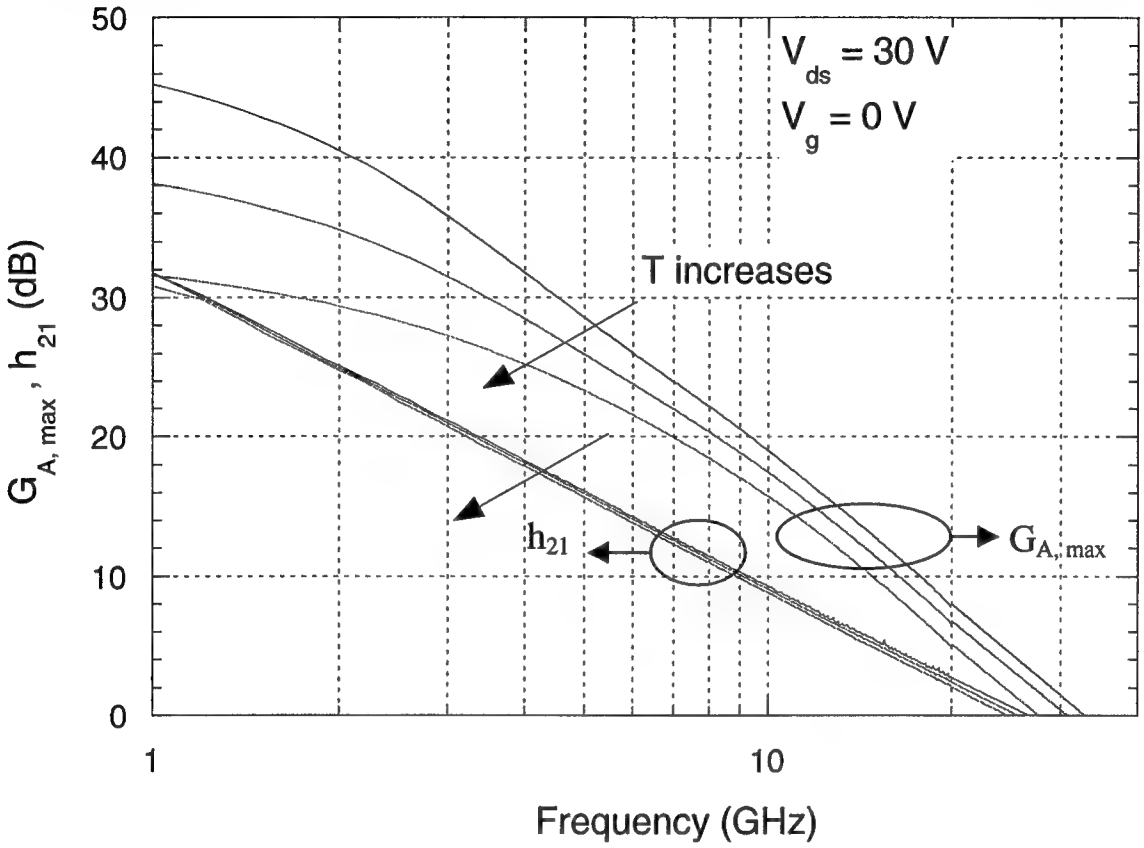
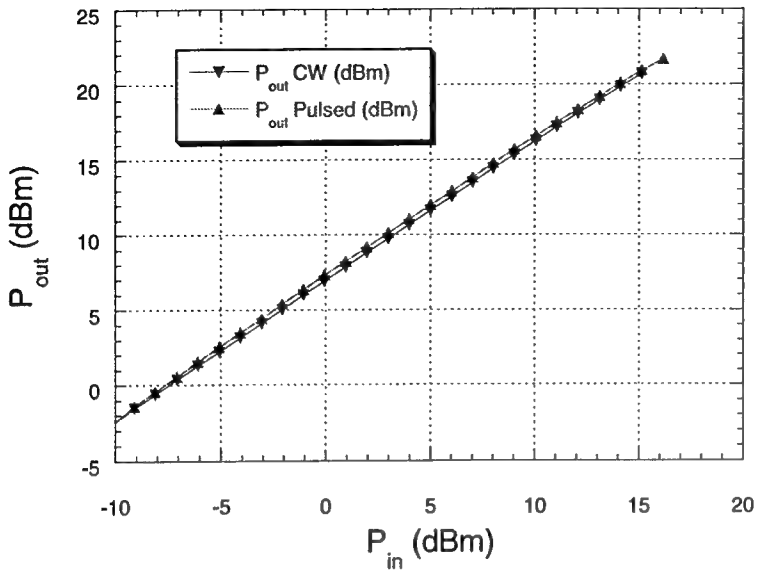


Figure 23. h_{21} and $G_{A, Max}$ versus Frequency at Various Temperatures.

Pulsed RF power measurements were made using the test setup shown in Figure 8. Figure 24 shows the results of pulsed RF power measurements on a 2-finger device into 50 Ohms termination at room temperature. The graph also includes measurement in a continuous mode. The pulse width on the gate side was fixed at 5 μs, the width on the drain side was 3 μs, and the RF pulse was centered with the drain pulse, it with was fixed at 2 μs. We observed that the device performance slightly improved under these pulsed conditions.



Period = 100 µs
V_g = 0 V
V_{ds} = 30 V
I_{ds} pulsed = 150 mA
I_{ds} CW = 130 mA
Freq. = 10 GHz
Into 50 Ohms

Figure 24. Pulsed/CW RF Power Results into 50 Ohms at 300 K.

Pulsed power measurement results described below were made with a 3.4µs pulse width on the gate side, a 3.2µs pulse width for the drain, and a 3µs pulse width for the RF signal. The RF input signal frequency is 10 GHz. Measurements were made at various test fixture temperatures. DC-IV curves of the device used for this RF characterization are shown in Figure 25. While the absence of negative slope in $I_{DS}(V_{DS})$ at V_G = -2V signifies a mode of operation free of heat, the negative output conductance for V_{DS} greater than 12 V at V_G = 0 V indicates that the device is self-heating. RF power measurements were carried out at a gate bias of 0 V and –2V at V_{DS} = 35 V in order to check the influence of self-heating under various classes of operation of the device. Figure 26 shows the results at V_{GS} = 0V and V_{DS} = 35V under continuous and pulsed condition. It appears that at this 10 GHz operating frequency, the gains (G_P, G_T) of the device remain the same under pulse and continuous mode of operation. However, as predicted by IV characteristics, the drain current is higher under pulse conditions, suggesting a decrease of the power added efficiency under pulse mode of operation.

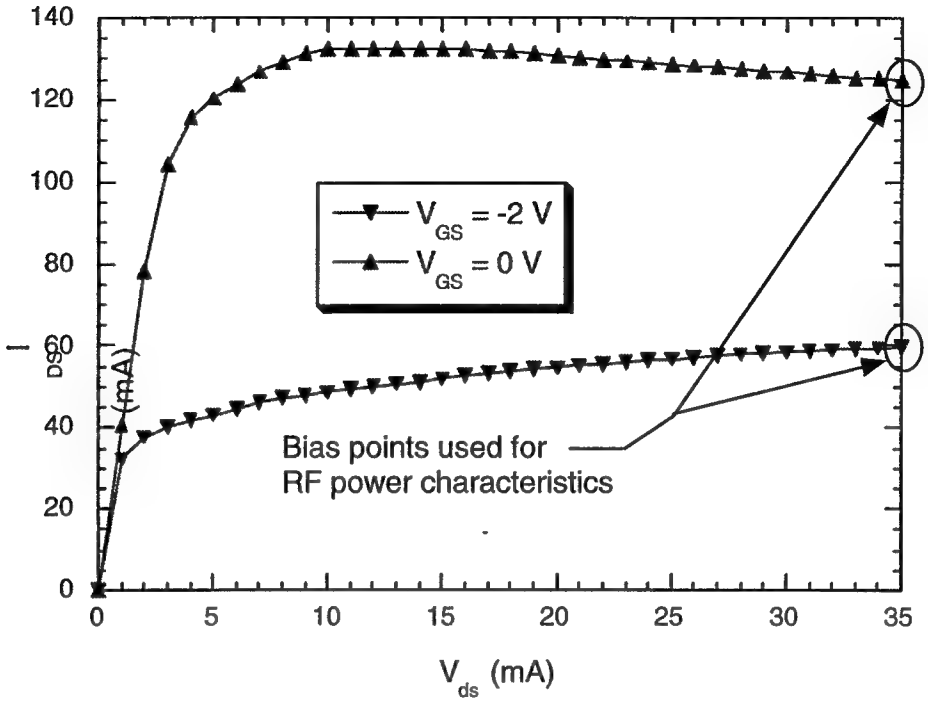


Figure 25. DC-IV Curves of the Device used for RF Characterization.

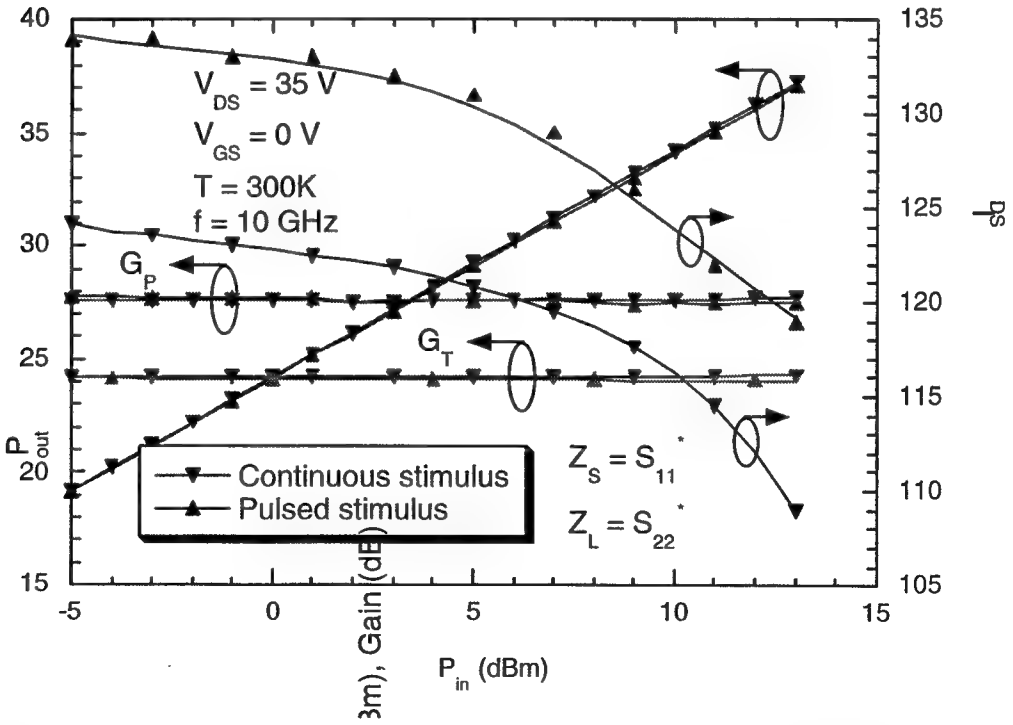


Figure 26. . Pulsed RF Power Measurement Results into Conjugate Match at 10GHz.

Figure 27 shows the RF power results at V_G = -2V and V_{DS} = 30V. At such bias conditions we observed from IV curves that self-heating is negligible. The power gain measured under continuous and pulsed mode remains similar, however the drain current is observed to be less important under pulsed condition when the RF power at the input of the DUT is less than 16 dBm, suggesting an improvement of the power added efficiency under pulsed conditions of operation at low RF power. By reducing the temperature of operation down to 100K the power gain of the device is enhanced, and the drain current is reduced when the applied RF power at the input of the device does not exceed 13dBm. Similar trends with the temperature are observed under continuous mode of operation.

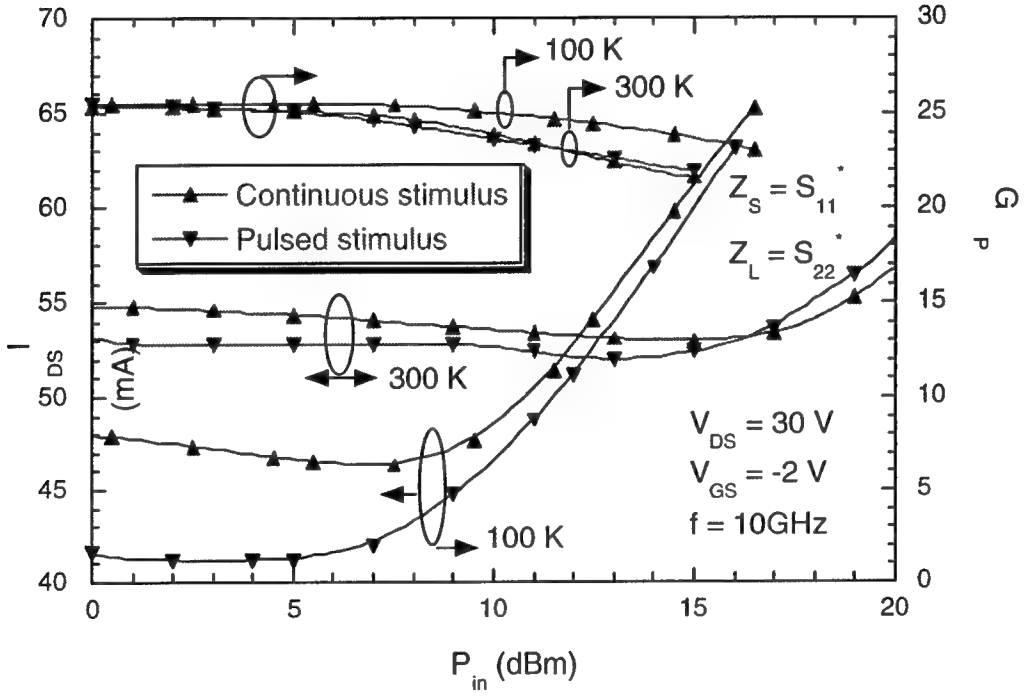


Figure 27. Pulsed RF Results into Conjugate Match at 10GHz, V_{DS}=30V, V_{GS}= -2V.

GTRI made extensive measurements on Cree Inc. devices and found them to be predictable and rather easy to probe. Most of our measurements concentrated on large signal characteristics to determine output power, power added efficiency and gain. Figure 28 shows a plot of output power as a function of input power on a two-finger device having a gate width of 250 microns. These measurements were made at 10 GHz using both CW and pulsed conditions. The pulse timing conditions are shown in the Figure and consist of a gate bias pulse of 5 microseconds, a 3 microsecond drain pulse center in the gate pulse and a input signal pulse of 2 microseconds also centered as shown in the Figure. Source and load tuners were set to 50 ohms in this particular measurement.

This Figure shows that for small devices, self-heating is not a problem under nominal RF conditions and the CW output power and pulsed output power are similar. Note in this case we have not driven the device very hard and the gain is not compressed appreciably.

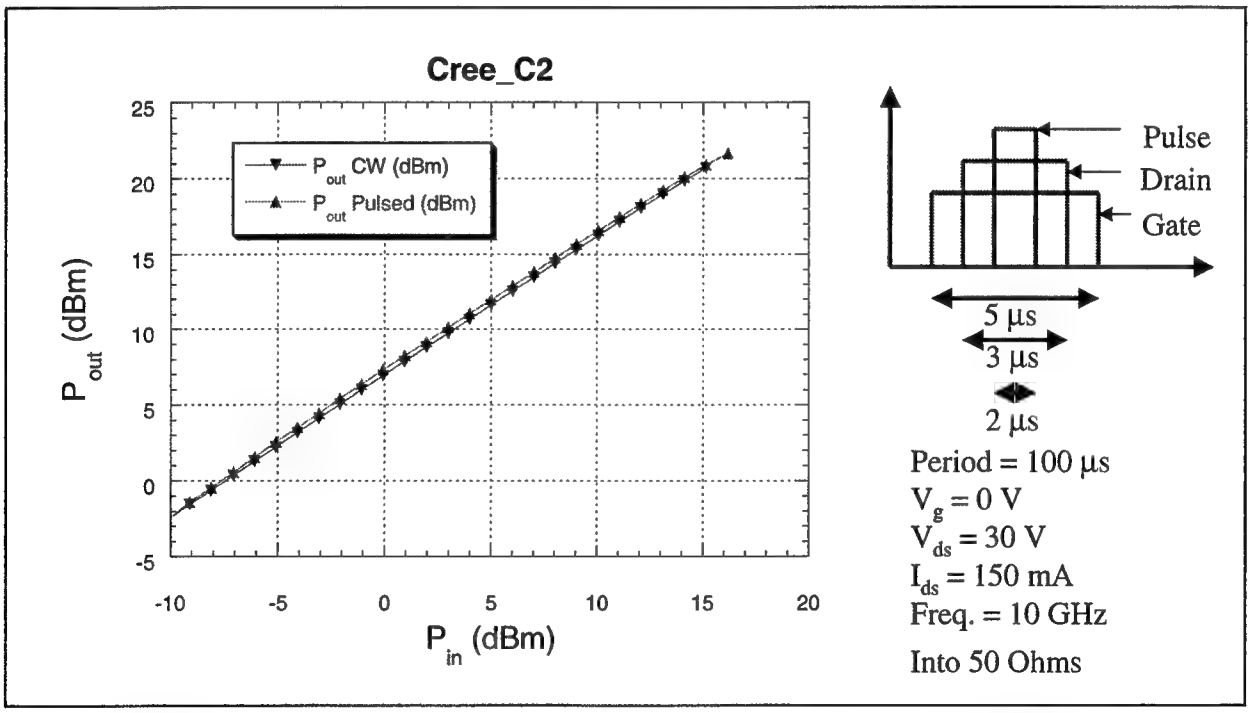


Figure 28. P_{out} Vs. P_{in} on 0.25 mm Device Input and Output Loads Set to 50 Ohms.

Figure 29 is a plot of output power as a function of input power for various temperatures under both pulsed and CW conditions. The plot shows increased gain and output power at lower temperature as expected.

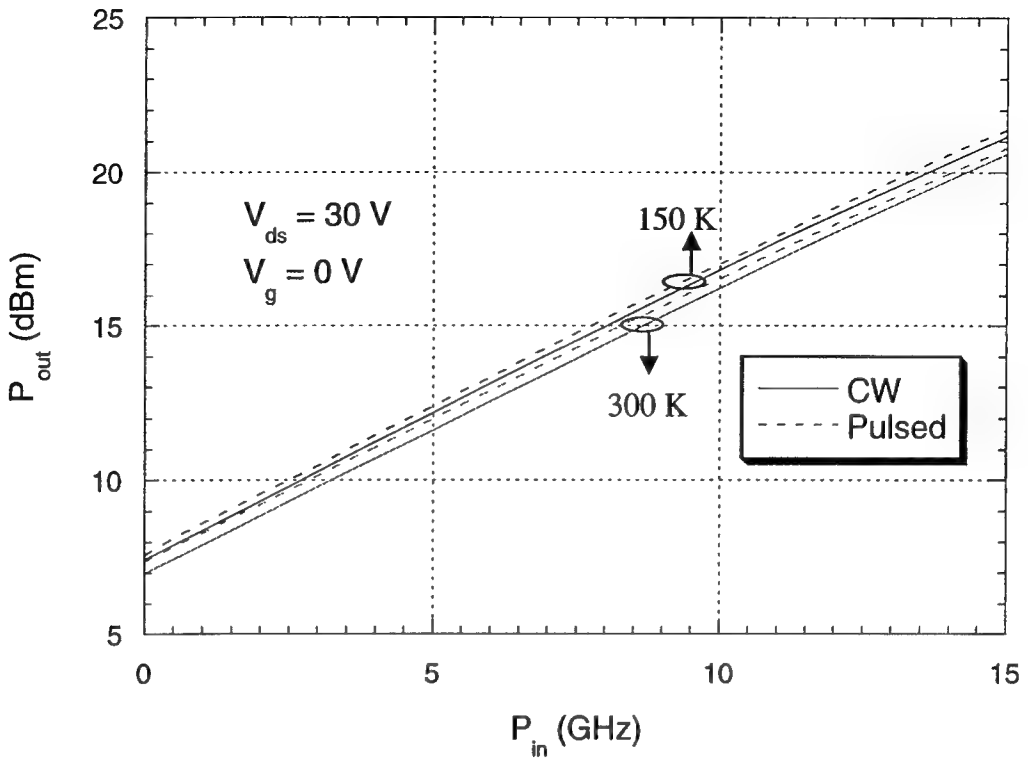


Figure 29. P_{out} Vs. P_{in} on a 0.25 mm HEMT under Pulsed and CW at Two Temps.

Pulsed load pull results for both 250 micron and 1.5 mm devices are described in this section. Figure 30 shows the I-V characteristics and bias points for subsequent load pull testing on a 250-micron gate width device. Table 1 shows the bias and load conditions.

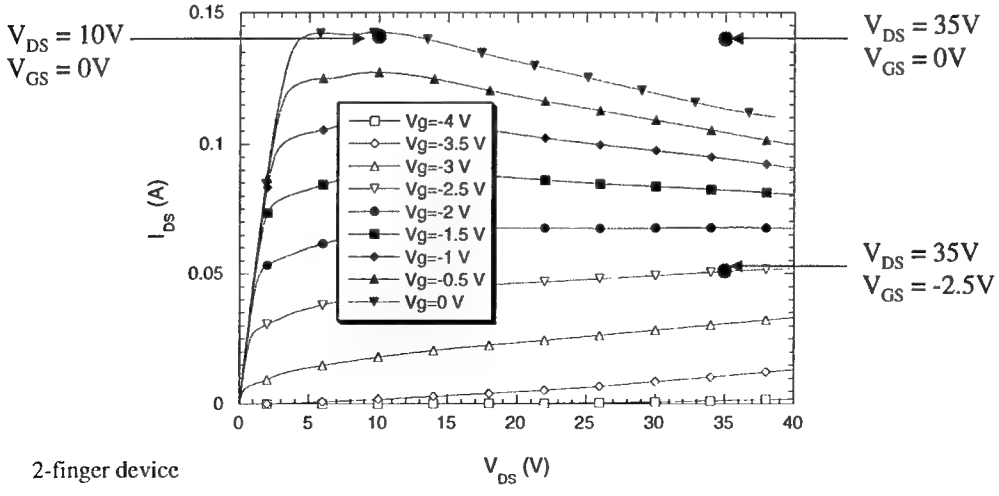


Figure 30. I-V Characteristics and Bias Points for Subsequent Load Pull Testing.

	VDS = 35V VGS = 0V	VDS = 35V VGS = -2.5V	VDS = 10V VGS = 0V
Γ_{Source}	0.743 < 91.60	0.6435 < 105	0.59 < 111.16
Γ_{Load}	0.431 < 43.74	0.634 < 43	0.376 < 46.5

Table 1. Bias, Source and Load Conditions for Measurements on a 250 Micron Device.

Figure 31 shows the response of this device at a gate bias of 0 volts. Nominal small signal gain is 14 db and the output power under 4 dB of gain compression is 29 dBm. Figure 32 shows the results for a gate bias of –2.5 volts. Small signal gain is slightly higher and the output power is also higher. Figure 33 show the results at a drain voltage of 10 volts.

Figure 34 shows a separate measurement at 8 GHz on a 250 micron device and includes power added efficiency. As shown in the plot, these devices are providing 4W/mm of output power.

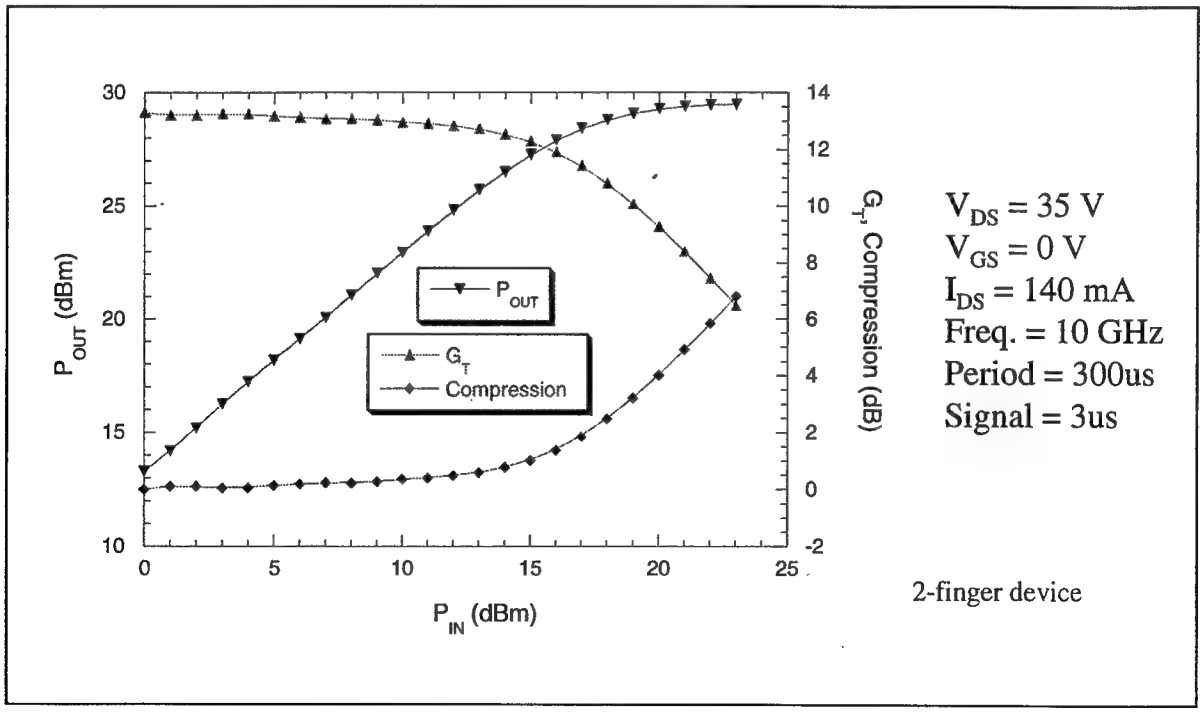


Figure 31. Output Power, Gain and Gain Compression at Vgs =0 Volts.

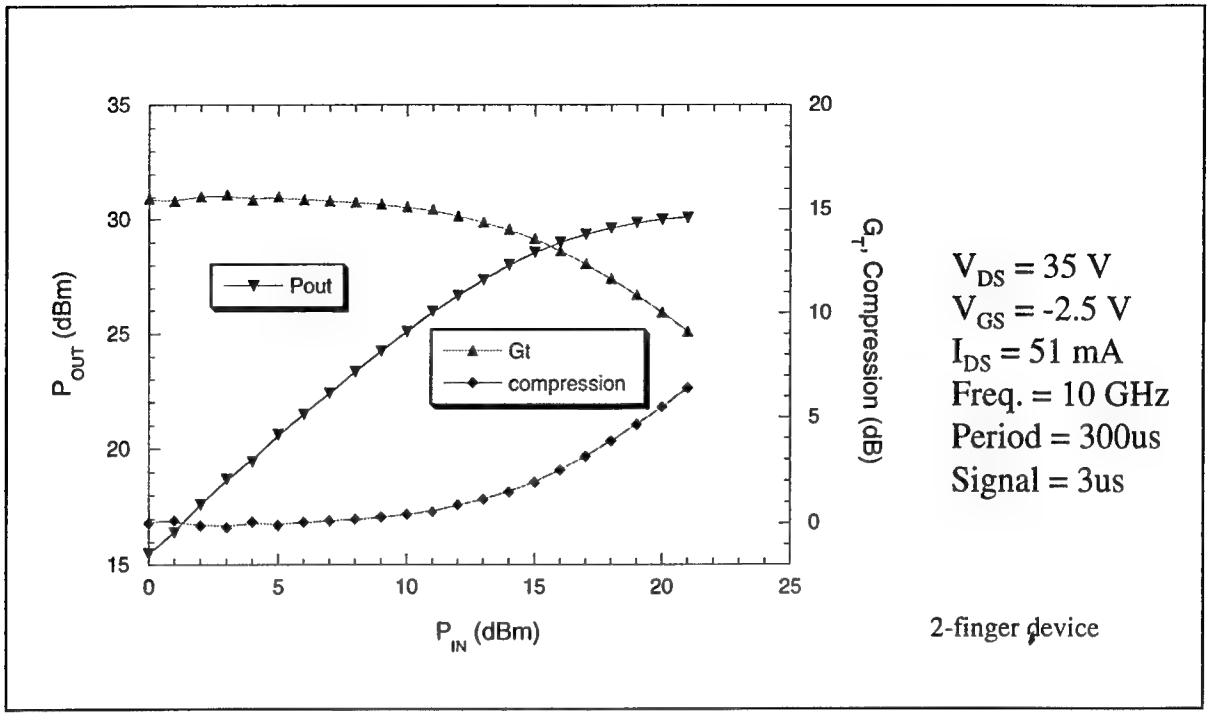


Figure 32. Output Power, Gain and Gain Compression at Vgs =-2.5 Volts.

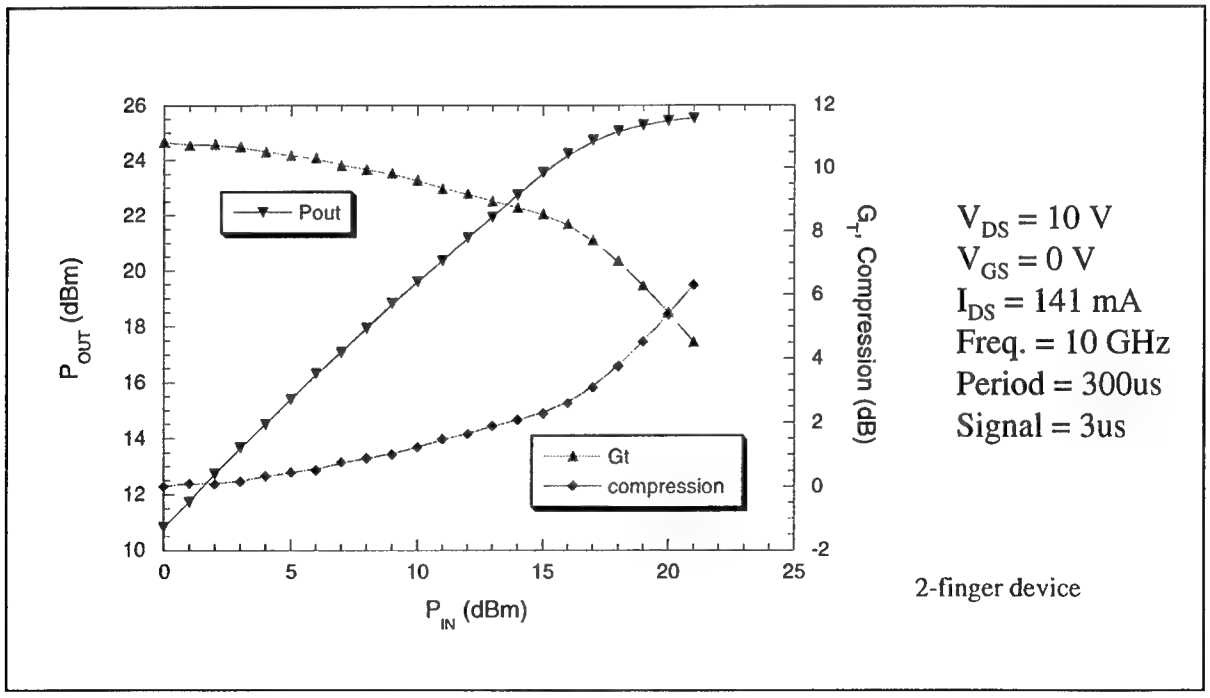


Figure 33. Output Power, Gain and Gain Compression at Vds = 10 Volts.

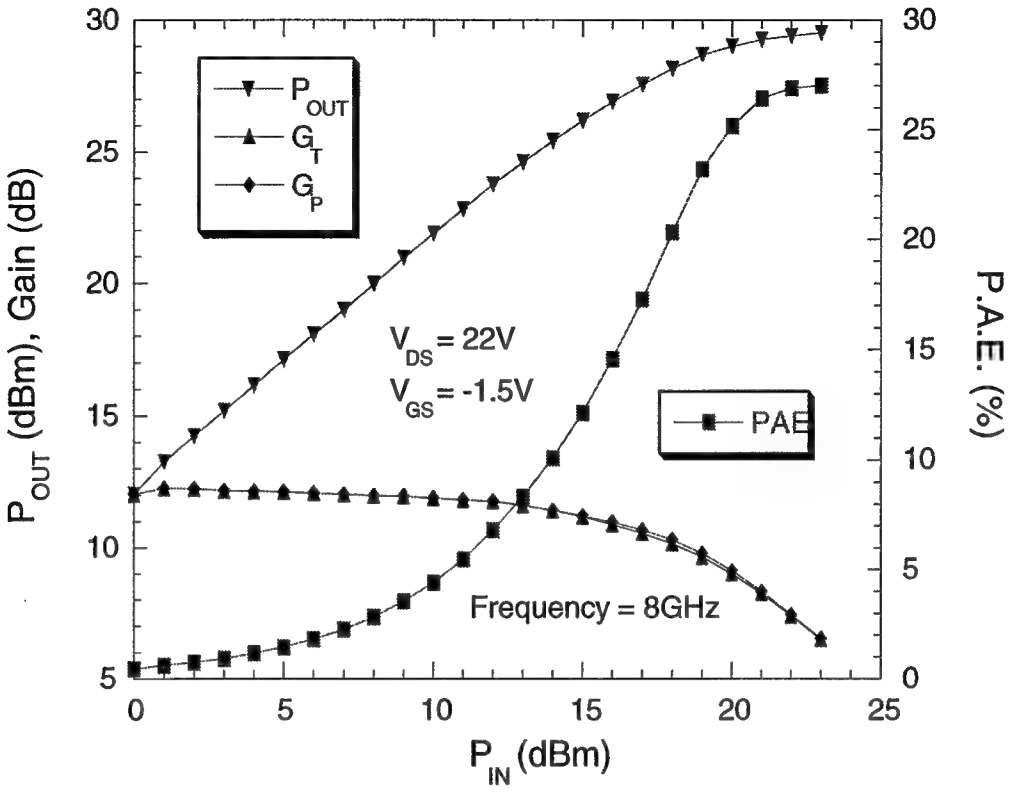


Figure 34. Pout, PAE and Gain at 8 GHz on a 250 Micron Device.

Large signal characterization was also performed on 1.5mm devices. Source and load gamma plots as shown in Figure 35 were made to determine the optimum conditions for maximum output power. In this particular case, the drain voltage was fixed at 35 volts and a pulsed input signal of 28dBm at 10 GHz was applied while tuning the source and load impedances. Figure 36 shows the output power and gain curves at an optimized impedance condition. Under these conditions the power density is approximately 5.3 W/mm.

GTRI/ECE was successful in measuring all of the Cree Inc. devices and their performance was found to be better than predicted by Cree. We were able to measure these devices under large signal conditions without any catastrophic failures. Some dc current instabilities were observed and are discussed later in this report. These instabilities did not cause any problems with our characterization, but could be a problem in the design and development of GaN based MMICs. GTRI has discussed this we Cree and they concur that additional work is needed to stabilize these devices. Advanced surface passivation may solve this problem.

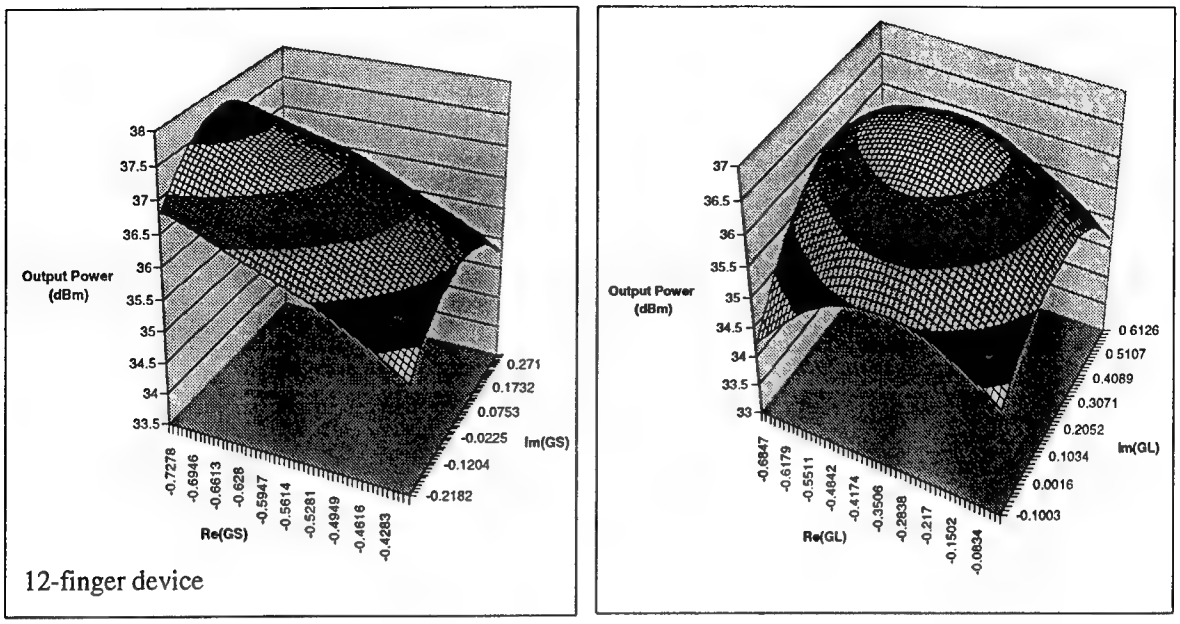


Figure 35, Source and Load Gamma Plots for a 1.5mm Device at 10 GHz.

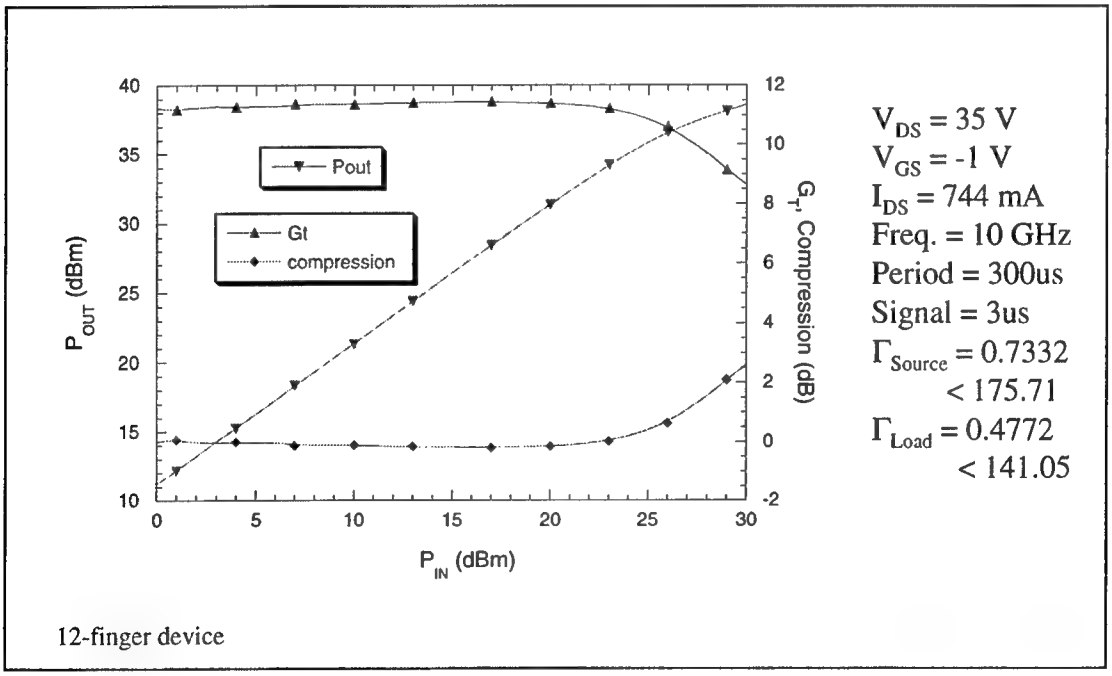


Figure 36. Output Power Gain and Gain Compression for a 1.5mm GaN HEMT at 10 GHz.

4.2 Cornell Devices

Dr. Richard Shealy provided GTRI with GaN HEMTs produced at Cornell on SiC substrates. Cornell uses an AlN nucleation layer during the MOCVD growth process. Upon initial dc characterization we observed a kink in the IV characteristics as shown in Figure 37. Sebastian Nuttink, Georgia Tech ECE, proposed that the kinks were due to a floating body effect as a result of the highly insulating buffer layer.

GTRI held discussions with Dr. Shealy and he arrived at what he termed "interesting conclusions" after reviewing data on approximately 50 runs. Some his conclusions are listed below and trend to support Georgia tech floating body effect theory.

1) HEMTs grown on sapphire with a GaN buffer (no AlN in structure) show kinks if the GaN buffer is insulating (1e8 ohm-cm has been measured on Cornell's undoped GaN). However if the nucleation process is off, then there is buried charge in the buffer (presumably from polarization effects) and the kinks are not observed.

2) On SiC with the GaN buffer (no AlN) Cornell does not observe these kinks and they observe high gate leakage (~ 1mA/mm) which limits the drain bias to roughly 30 volts. As GTRI observed, **on structures with an AlN sub buffer** (not the nucleation layer), Cornell fabricated 5 different growth experiments, and **each of them has kinks.**

3) Gate leakage (from the pads) or isolation problems seems to correlate well with the absence of kinks - unless the Schottky contact is degraded (by annealing or excessive self heating)

4) Accordingly, **Georgia Tech's assessment of the kinks is correct.**

If the GaN buffer is insulating and substrate conduction is avoided, then kinks appear. When insulating GaN results on top of the AlN, Cornell has shown on 5 runs of this type, that all show kinks. Furthermore, the AlN is not present on Cornell's sapphire structures and the kinks can be more pronounced.

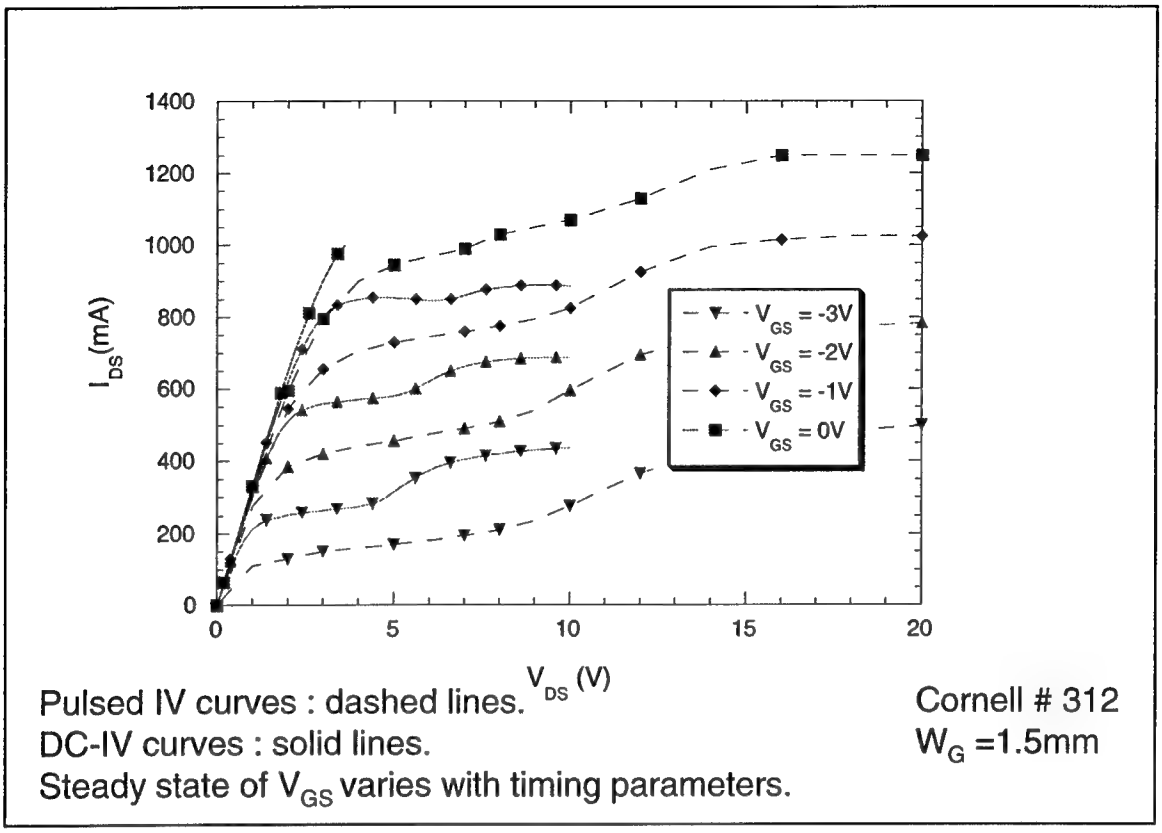


Figure 37. DC and Pulsed IV Characteristics for a 1.5mm Cornell Device.

The following Figures describe the results on the two Cornell devices that we characterized. GTRI/ECE performed DC/Pulsed IV, Time-dependent DC-IV, f_{max}, f_T evaluation, CW Large-signal characteristics, CW tuning @ V_{DS} = 20V, V_{GS} = -1V and CW/Pulsed IMD @ V_{DS} = 20V, V_{GS} = -1V. We also investigated gate a drain current stability as function of time. This data is included in a subsequent section.

We found that the Cornell devices have a F_T and F_{max} of approximately 30 GHz. based on small signal measurements. An output power density of 1.7 W/mm was observed on a 1.5mm device and the associated efficiency was 38% at a 2 dB compression point. These data were consistent with Cornell data supplied with the devices.

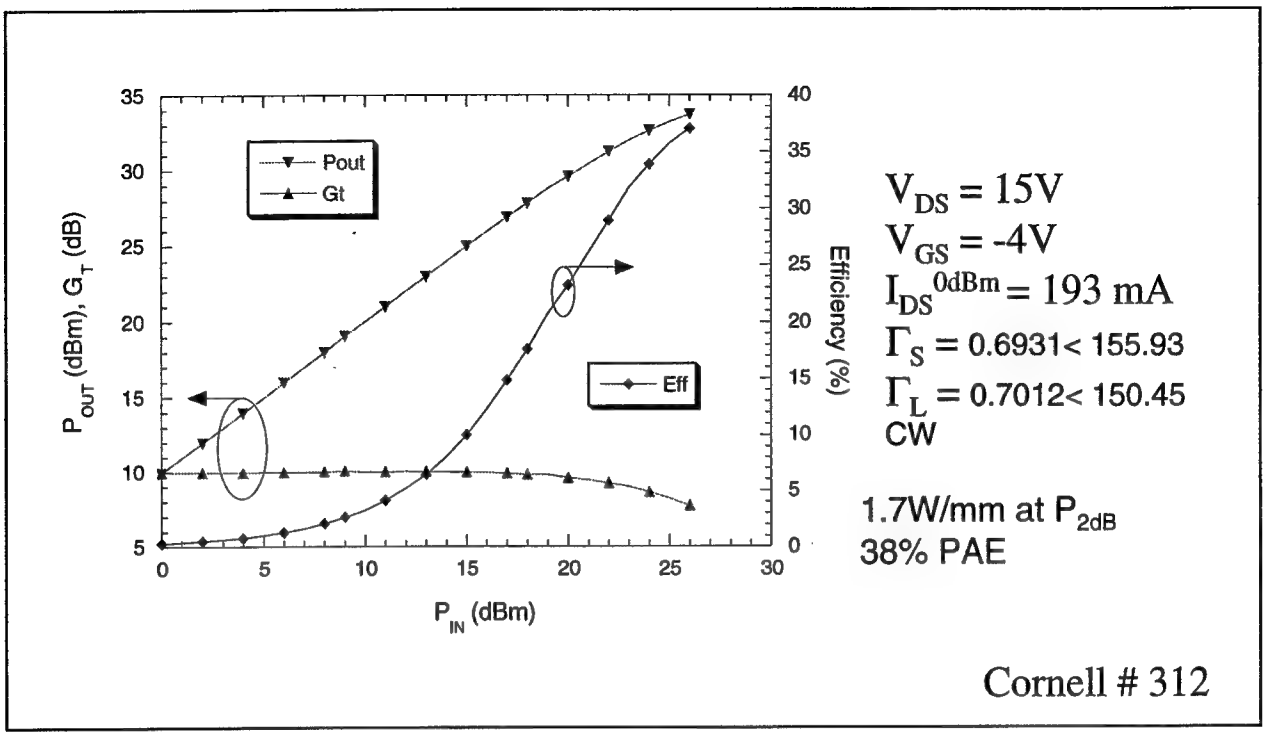


Figure 38. Output Power, Gain and PAE on Cornell Device 312.

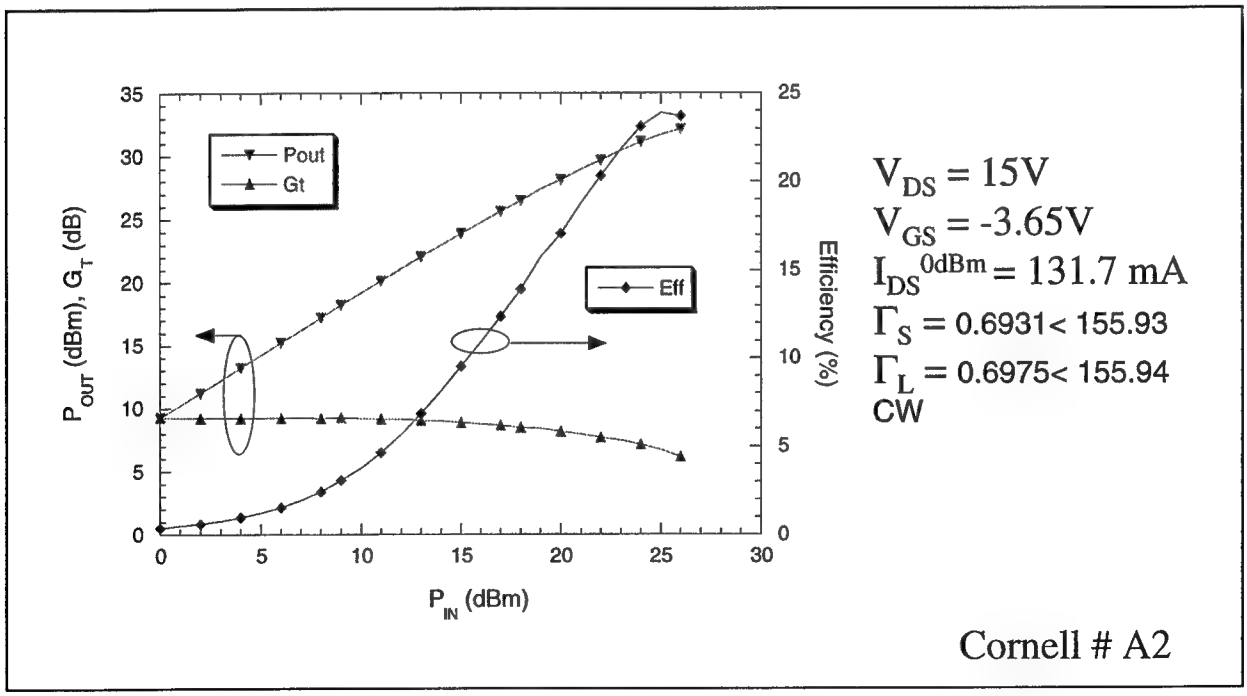


Figure 39. Output Power, Gain and PAE on Cornell Device A2.

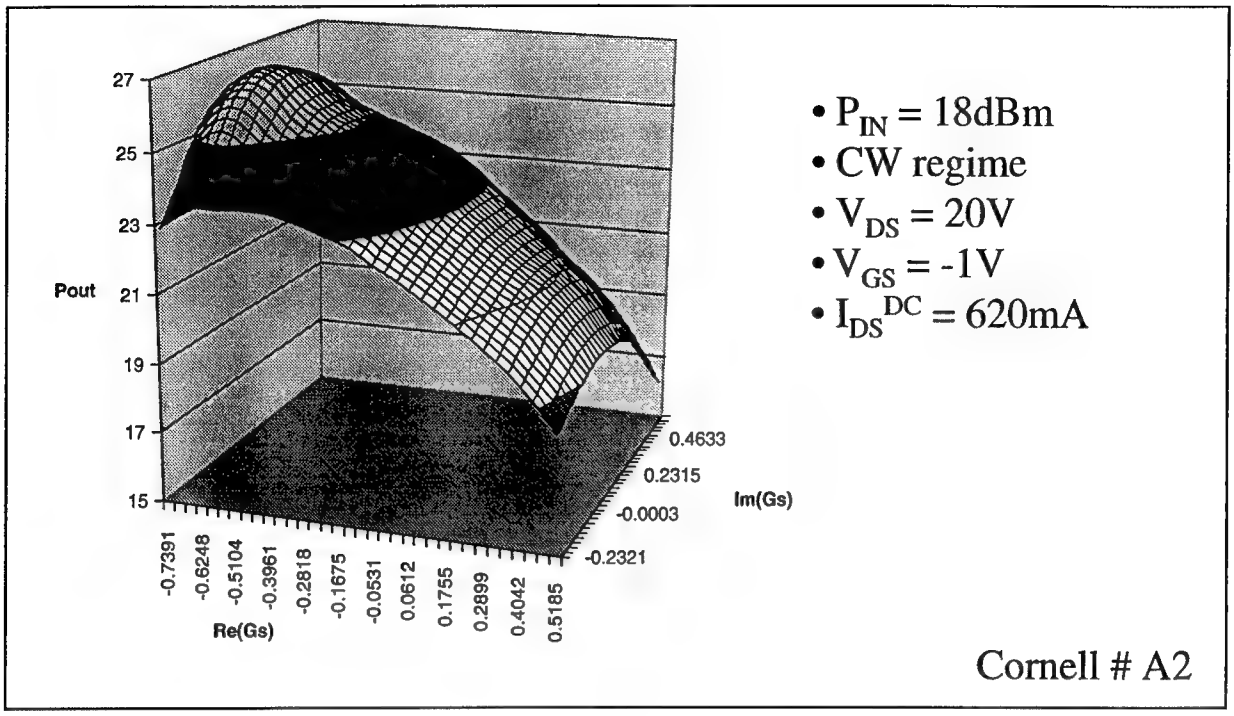


Figure 40. CW Tuning Characteristics for Cornell Device A2.

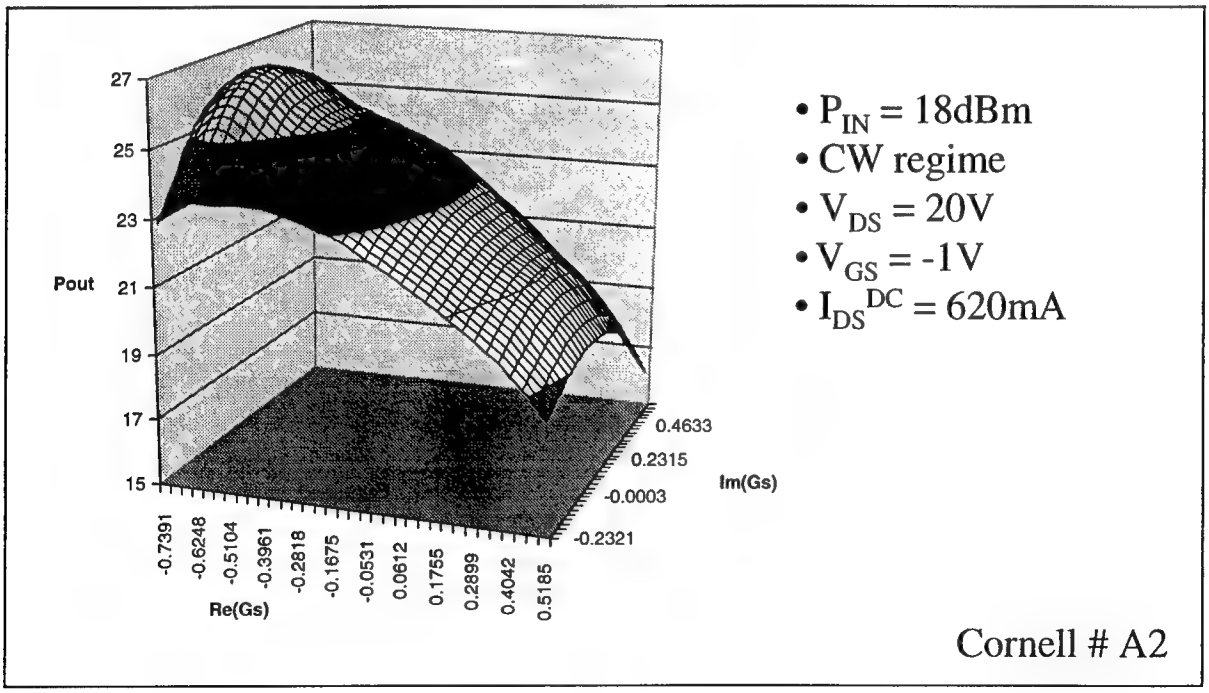


Figure 41. Pulsed Inter-modulation Distortion Characteristics.

4.3 Cree Lighting

Primit Parikh, of Cree Lighting provided a quarter wafer having devices of five different types with gate widths of 100, 250, 300, 2100, 3200 microns respectively. The 2.1 mm and 3.2 mm devices were not full gate width devices because the air bridge step, that connects the sources, was not completed on this particular wafer. Cree Lighting's large signal testing at 4 -10 GHz demonstrated 6 W/mm output power with 30-40 % PAE at 35-40 Volts drain bias.

GTRI measurements on these devices confirmed state-of- the-art performance on small gate width devices. Maximum power density was found to be approx. 5W/mm on 250 micron devices at 4-5dB gain compression at a drain bias of 35V. Maximum power added efficiency (PAE) was found to be 37% on a 250 micron device. Device to device performance varies over the wafer, even in the same vicinity and gate pads are very sensitive to probing and degrade quickly. The air bridge step would probably add additional metal to the gate pads and make them more robust.

Figure 42 shows the layout of these devices. And the following figures show our measurement results.

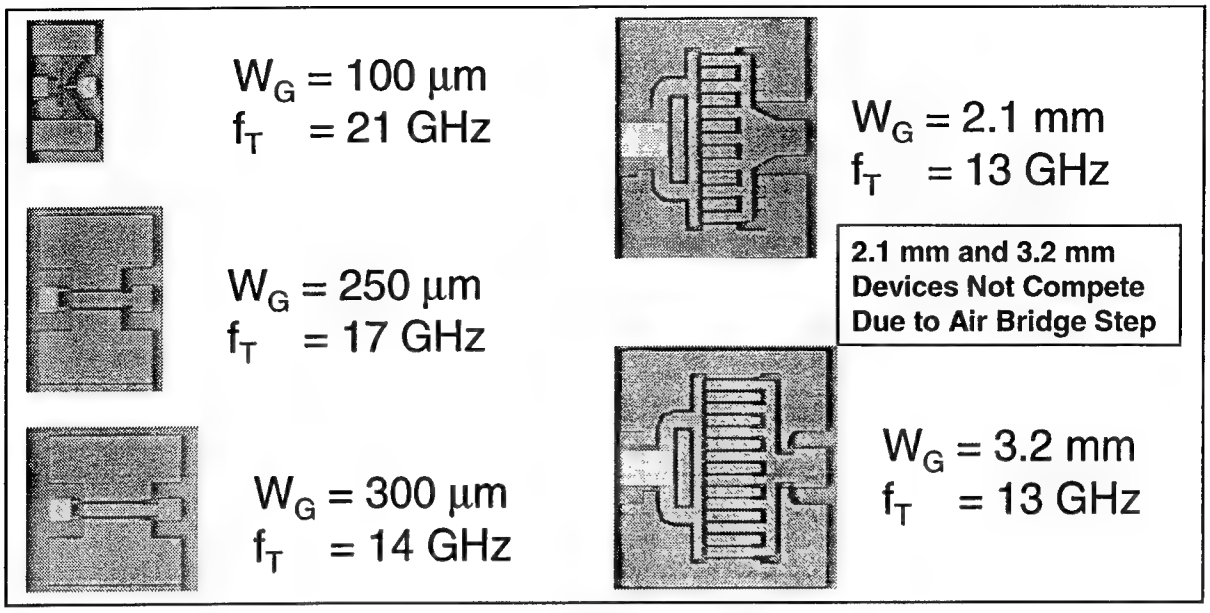


Figure 42. Cree Lighting Device Layouts.

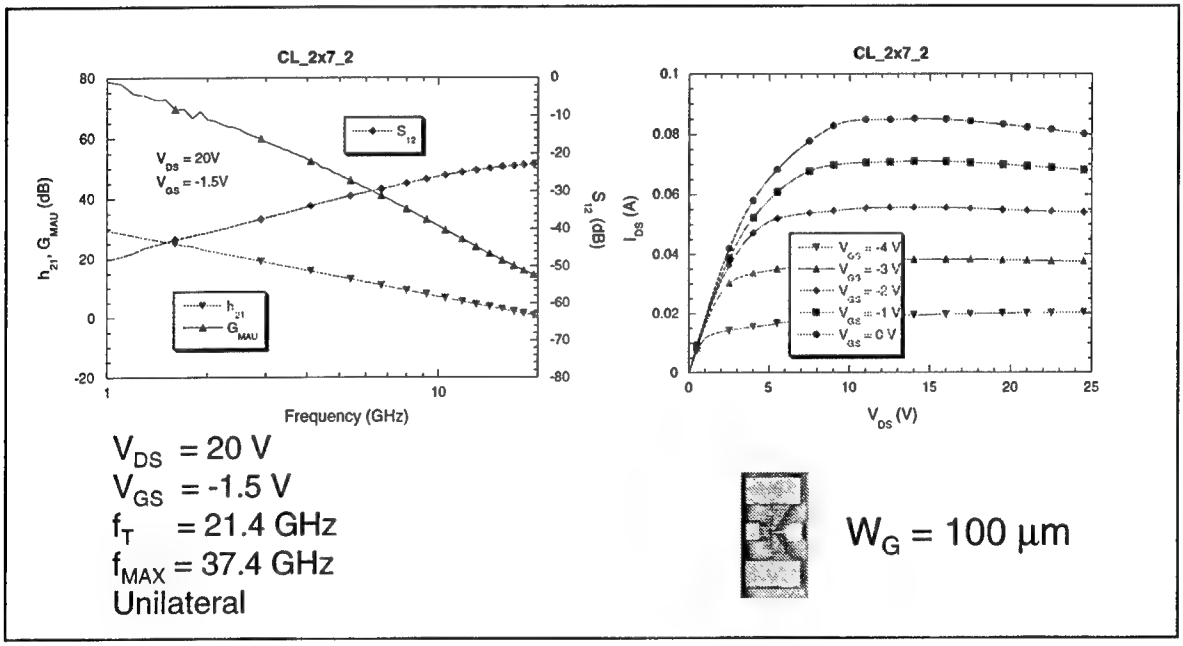


Figure 43. IV and Small Signal Results on a 100 Micron Device.

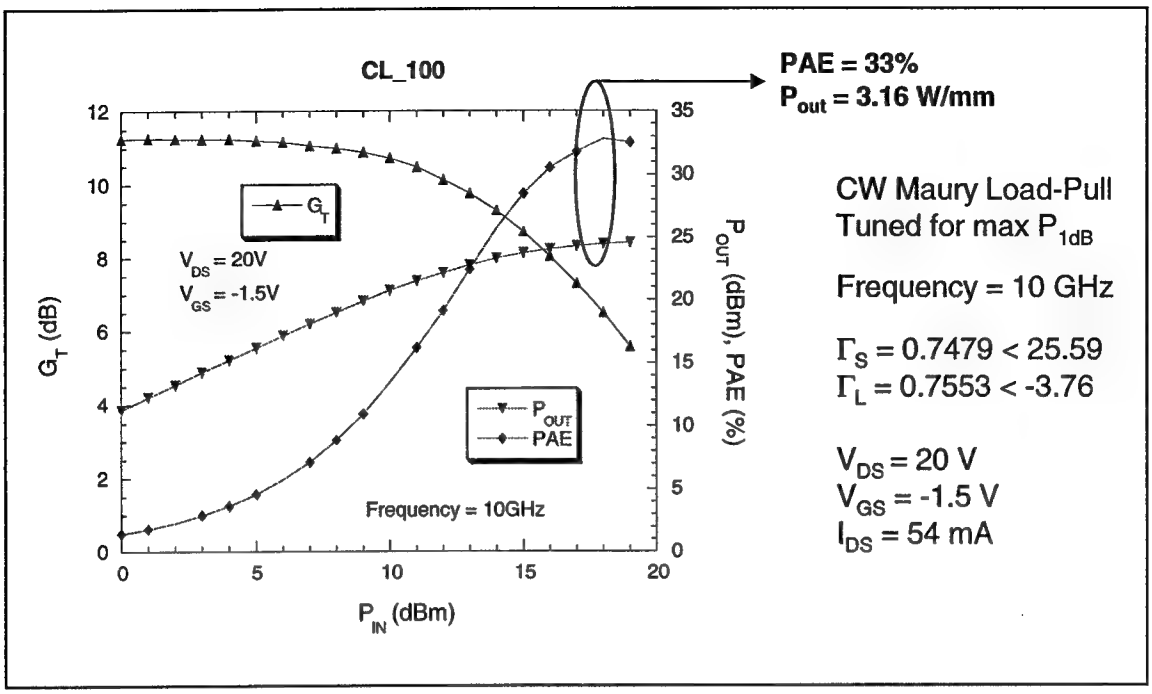


Figure 44. Output Power, Gain and PAE of a 100 Micron Cree Lighting Device.

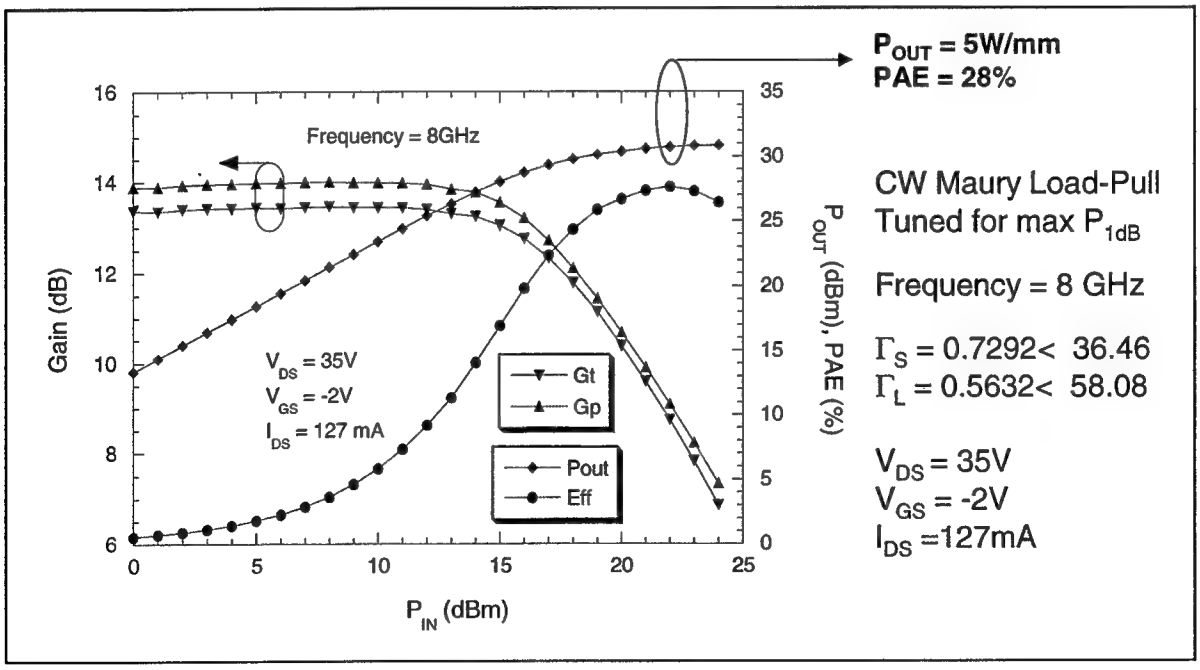


Figure 45. Characteristics of a 250 Micron Device Tuned for Maximum Power Density.

5. DC Instabilities

In response to reports that the DC current varied up to +/- 2% or so over time with no change in bias, GTRI performed preliminary tests on Cree Inc. We found that the drain current changes about 1% after 10 minutes when biased at Idss. An Agilent 4155 semiconductor parameter analyzer was used to provide the bias and to monitor the currents. Sample rate on the HP4155 was 1/sec. Figure 46 shows the results of this test at Idss and indicates that most of the change occurs in the first two minutes and then tends to stabilize on these devices. The most profound change was in Igs at the high drain bias condition. We observed a nominal 28% change in Igs after ten minutes.

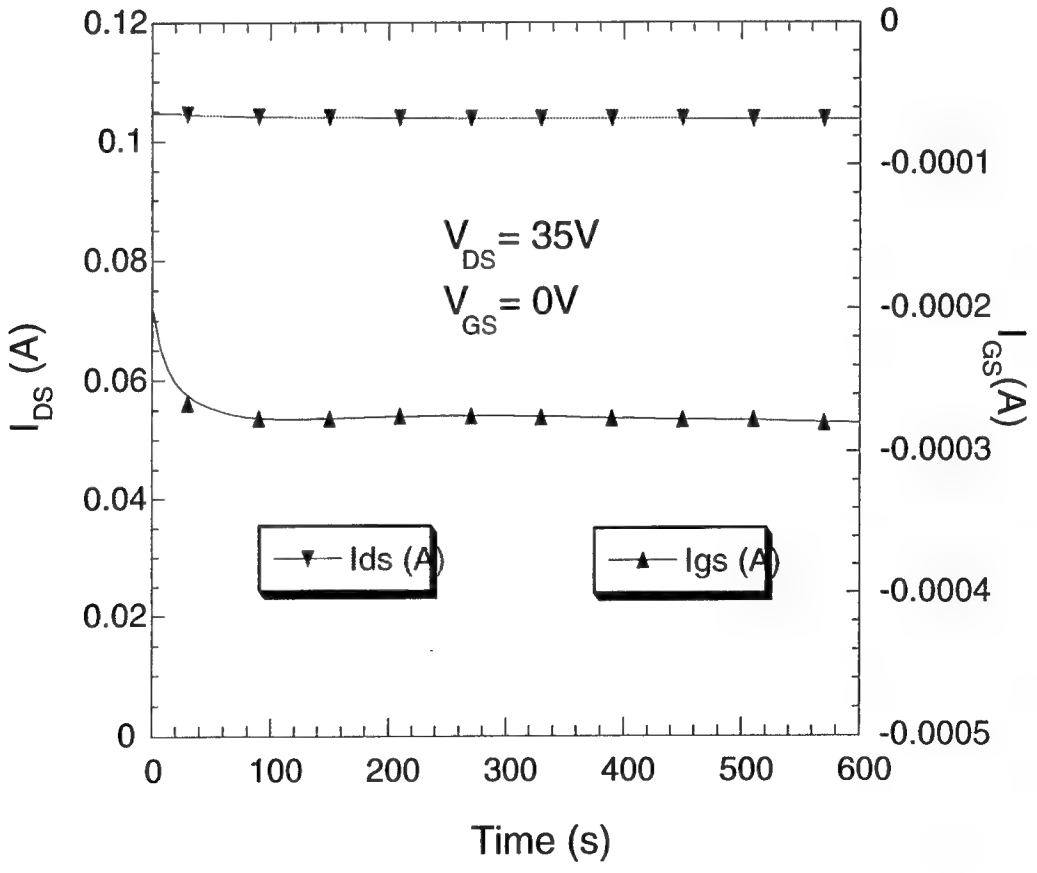


Figure 46. Change in Drain/Gate Current with Time for Cree GaN HEMT (biased at Idss).

GTRI also biased devices at one-half Idss and saw a nominal 3% change in drain current and a 2% change in gate current. Figure 47 shows the trends in Idss and Igs as a function of time for this bias condition. In this case, the trend in drain current was increasing rather than decreasing as observed when bias at Idss. Gate current tended to decrease as observed when biased at Idss.

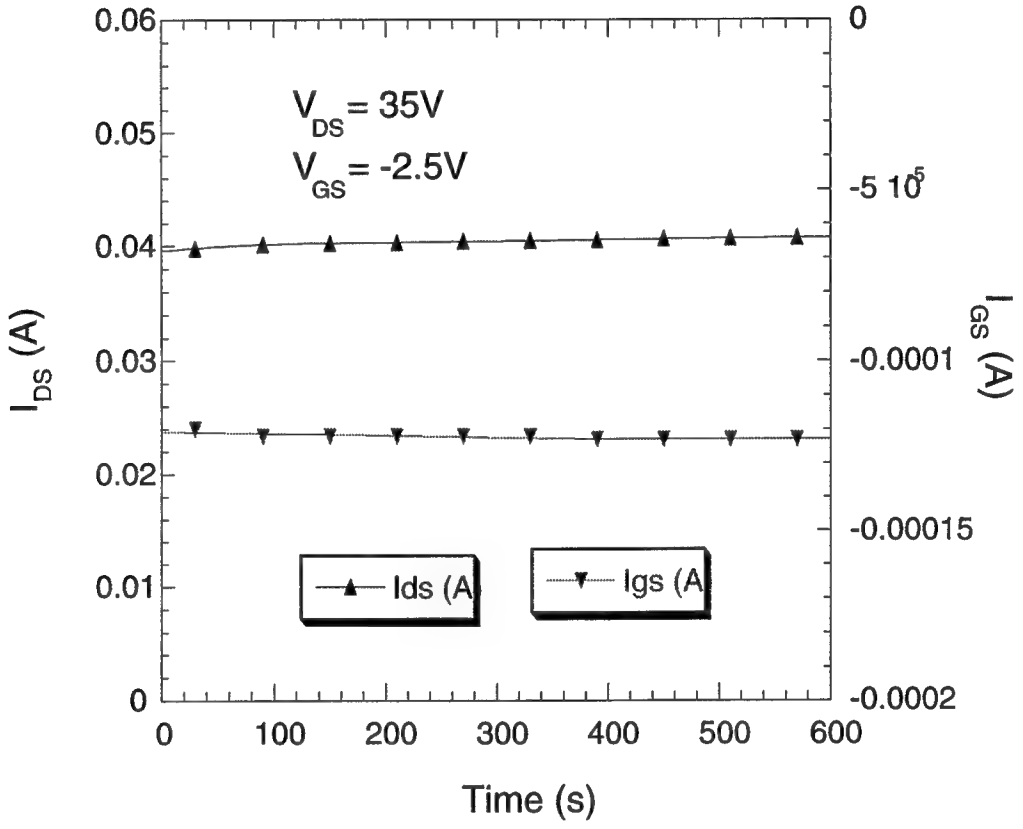


Figure 47. Change in Drain/Gate Current with Time for Cree GaN HEMTs (V_{GS} = -2.5V).

GTRI/ECE performed the same measurements of a device supplied by Cornell and observed a change in the drain current of 4.6% in five minutes; however the gate current was

relatively stable and low compared to the Cree Inc. devices. It should be noted that the drain bias on the Cornell device was 10V compared to 35 V for the Cree devices.

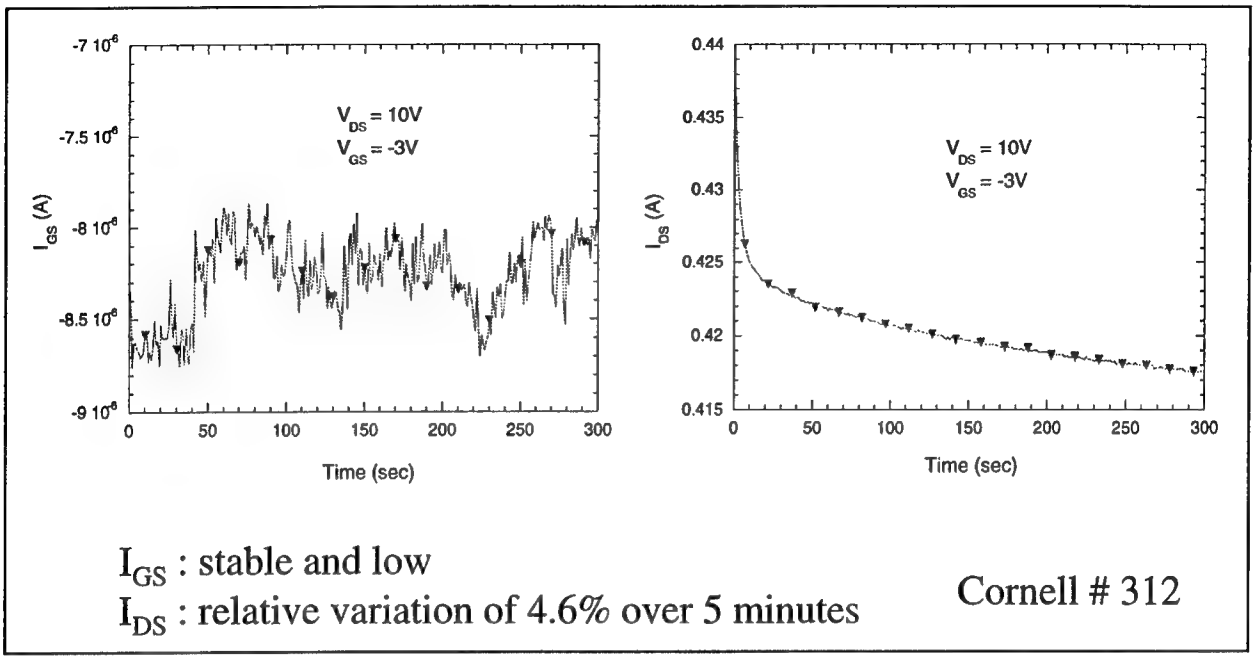


Figure 48. DC Stability Characteristics for Cornell Device 312.

Drain and gate current instabilities are likely due to several sources. A likely source is surface state charge that may be influenced significantly by the higher field in GaN devices compared to GaAs devices. Clearly this instability need s to be solved in order to design and fabricated reliable GaN-based MMICs. Cree and Dr. Shealy's group at Cornell agree with our observations and conclusions that this sis a problem that need to be solved.

6. Substrate Effects

Anomalies in the DC IV characteristics were discussed in Section 4.2. These anomalies have been theorized to be due to floating body effect associated with having a high resistivity buffer layer in the device structure. Figure 49 is a cross-section of an AlGaN/GaN HEMT layer structure that exhibits a kink effect in the dc IV characteristics. The body of the HEMT is formed on an AlN layer. Details of this type of structure are discussed in [1]. At 300K, the bandgap of AlN is 6.2ev, its high frequency dielectric constant is $\varepsilon_r^{AlN} = 4.77 \cdot \varepsilon_0$ [2], and its resistivity, ρ^{AlN}, is greater than $10^{14}\Omega.cm^{-1}$. These semiconductor properties suggest that the body of these devices is formed on a reasonably good insulator. Since no contacts are fabricated between the body and the source, some properties similar to thin-film SOI ($\varepsilon_r^{SiO_2} = 2.4 \cdot \varepsilon_0$, $\rho^{SiO_2} > 10^{14}\,\Omega.cm^{-1}$) can be expected [3-7].

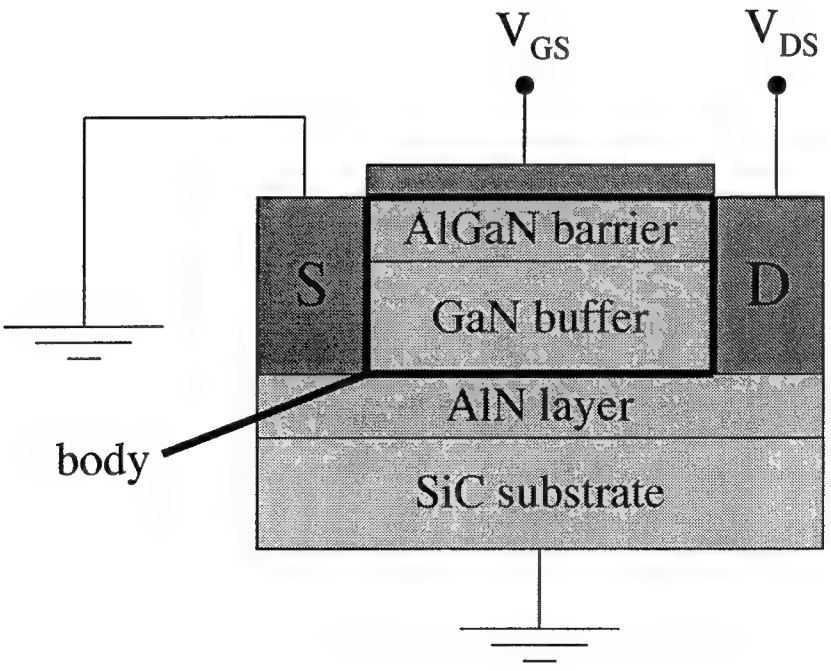


Figure 49. Representative GaN HEMT Layer Structure.

When no contacts are fabricated between the body and the source, a kink is present in the current characteristics due to the existence of a body-to-source voltage V_{BS} that modifies the threshold voltage V_{TH} [3]. As shown in Figure 50, a kink is observed in the current characteristics of these HEMTs. This kink has already been measured in similar AlGaN/GaN devices [8,9] but has not been studied. When trapping effects are dominant, adding a delay between each drain voltage sweep gives time for trapped carriers to relax, and current characteristics become kink-free. In those devices, even a delay of 120 seconds does not yield a kink-free characteristic. In addition, pulsed IV measurements are performed and results still exhibit a current kink ruling out the possibility of traps being the origin of this perturbation.

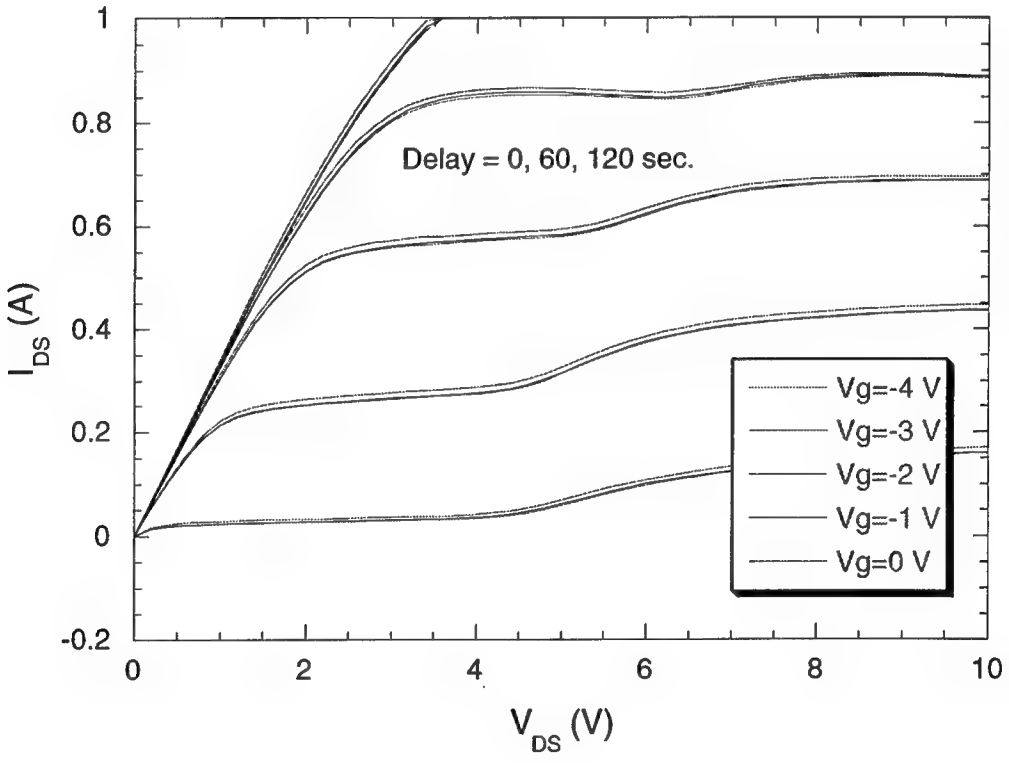


Figure 50. DC IV Characteristic Showing a Kink Effect.

Georgia Tech derived a method from SOI techniques and applied it to extract the off-state floating body (FB) voltage (V_{BS}). Coherence of the results obtained confirms that FB effects are effectively present in this type of device. In addition, IV characteristics have been measured on AlGaN/GaN devices with different layer structure. HEMTs, grown on sapphire with a GaN buffer (no AlN), show kinks if the GaN buffer is insulating (a resistivity of $10^8\Omega.cm^{-1}$ has been measured on undoped GaN). If the nucleation process is off, buried charges are present in the buffer, presumably from polarization effects, and the kinks are not observed. Therefore, the floating-body assessment can be extended to other AlGaN/GaN HEMTs if the GaN buffer layer is insulating and substrate conduction is avoided.

Georgia Tech prepared a detailed paper regarding this phenomenon in collaboration with Cornell. This paper is included as an Appendix.

7. Thermal Analysis

GTRI performed a thermal analysis on a material stack representative of one that likely would be used with GaN MMIC high power amplifiers. The materials stack was composed of:

- a two-finger GaN FET grown on SiC substrate modeled as (GaN active region = 4μm), (SiC substrate = 13mil)
- (AuSn solder = 1mil)
- and a (CuMoCu base = 80mil).

The temperature of the base plate was fixed at 20°C, and simulations were performed under pulsed and continuous conditions with a power density to dissipate of 5W/mm. RadTherm Thermal Analysis software was used for the analysis.

Fig. 8 shows the peak GaN surface (red), the GaN/SiC interface (blue) and the CuMoCu surface (green) temperatures for a series of 5ms pulses at 25% duty cycle. Timing parameters correspond to those that might be used in pulsed radar applications. A 30°C temperature drop in the thin GaN epi layer is reported, and the peak temperature is about 20°C lower than the continuous wave case (T_{CW} = 96°C).

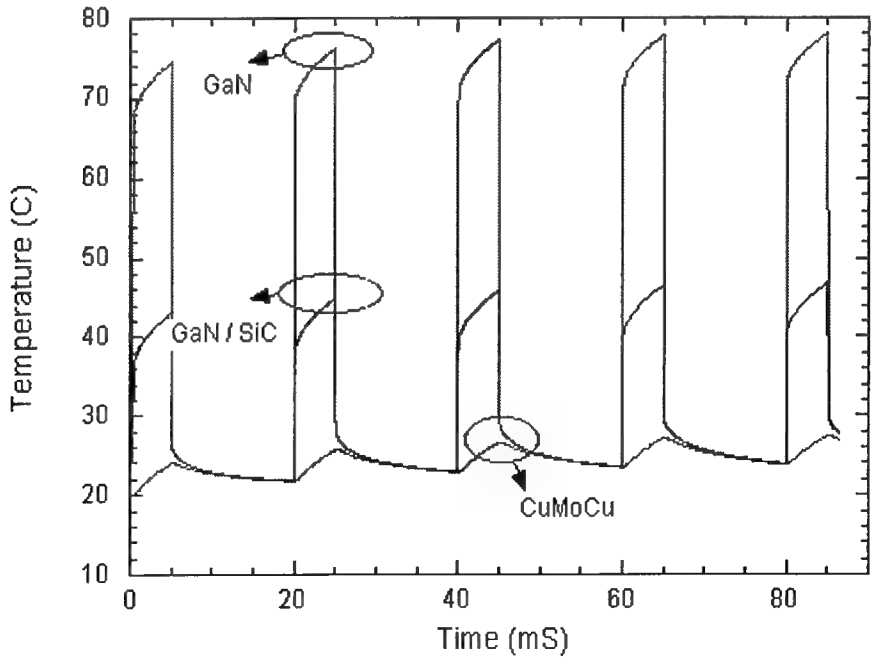


Figure 51. Thermal Analysis Results for a Standard Materials Stack - Pulsed Conditions.

8. Recommendations and Conclusions

In addition to detailed on-wafer measurements results of DC-IV, Pulsed-IV, and S-parameters, a novel pulsed load-pull system featuring reflected power measurements has been built and utilized to measure for the first time RF power characteristics of GaN HEMTs at various temperatures of operation under pulsed condition. These measurements allow the understanding of self-heating effects in GaN-based transistors and the possibility for device structure improvement resulting in better device performance. The measurement results give an in depth understanding of device behavior and are the basis for robust device modeling. A small-signal model that takes into account the device geometry for parasitic extraction has also been developed at different temperatures of operation. Work remains to make high power measurements on larger devices and to further investigate trapping effects.

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10. Appendix A- Publications

"Development of GaN Wide bandgap Technology for Microwave Power Applications", *S. Nuttinck, E. Gebara, J. Laskar. And M. Harris. IEEE Microwave Magazine, March 2002.*

"RF Performance And Thermal Analysis of AlGaN/GaN Power HEMTs in Presence of Self-Heating Effects", *S. Nuttinck, E. Gebara, J. Laskar, B. Wagner, and M. Harris. Submitted to IEEE MTT 2002, Seattle.*

"Measurements And Modeling of Floating Body Effects in AlGaN/GaN Power HEMTs", *S. Nuttinck, E. Gebara, M. Harris, and J. Laskar. Submitted to IEEE Trans. On Electron Devices, vol. ##, No ##, pp ##, ## ##.*

"Power and Noise characterization of AlGaN Power HEMTs in Presence of Self-Heating Effects", *S. Nuttinck, E. Gebara, M. Harris, and J. Laskar, IEEE Topical Meeting on Power Amplifier, San Diego, Sept.2001.*

"Study of Self-Heating Effects And Temperature-Dependent Modeling And Pulsed Load-Pull Measurements on GaN HEMTs", *S. Nuttinck, E. Gebara, J. Laskar, and M. Harris. IEEE Trans. on Microwave Theory and Techniques, vol. ##, No ##, pp ##, Dec. 2001.*

"Study of Self-Heating effects in GaN HEMTs", S. Nuttinck, E. Gebara, J. Laskar, and M. Harris. IEEE MTT_S, vol. 3, pp 2141-2143, Phoenix, June 2001.

DEVELOPMENT OF GaN WIDE BANDGAP TECHNOLOGY FOR MICROWAVE POWER APPLICATIONS

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I. INTRODUCTION

Solid-state amplifiers are replacing traveling-wave-tube-amplifiers (TWTAs) for microwave power applications. However, the low operating voltages of solid-state devices lead to a large device periphery resulting in high device and circuit complexity, reducing production yield and reliability. Wide-bandgap technologies like GaN can achieve power density 5 times higher than the one of conventional GaAs/InP based high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). This will ultimately result in reduced circuit complexity, improved gain, efficiency, and reliability. Both, military (e.g. Radar) and commercial applications (e.g. communication systems) will benefit from the development of this technology.

In order to provide a mature technology based on GaN, it is crucial to fully investigate wide-bandgap electronic devices and circuits. This includes the understanding of the device technology, of its reliability, and the development of circuits and system applications. Those needs are being addressed by the development of the adequate characterization systems, and the analysis and modeling of the measurement results. This is the basis for accurate high power microwave circuit designs that form the building blocks for larger systems. We present in this paper results of such investigation regarding AlGaN/GaN power HEMTs.

Section II presents a complete characterization of AlGaN/GaN power HEMTs. Measurements systems and results along with device modeling are presented. Section III discusses major issues regarding the device's reliability. It includes fabrication aspects, and thermal analysis. Finally, section IV addresses needs in term of circuit and system applications.

II. DEVICE TECHNOLOGY

AlGaN/GaN high electron mobility transistors (HEMTs) offer important advantages for high power applications due to the GaN wide bandgap [1-5]. GaN-based FETs offer power

densities in the few W/mm range, cutoff frequencies (f_T) above 20GHz, and maximum frequency of oscillation (f_{MAX}) beyond 25 GHz. However, the overall power present in GaN-based power FETs is large and cannot be completely dissipated throughout the substrate. As a consequence AlGaN/GaN HEMTs suffer from self-heating effects. Operating devices during a short period of time permits one to control the heat dissipation in a device. Based on this assessment, pulsed-IV, pulsed S-parameter, and pulsed load-pull systems [6,7,8,9] have been implemented in order to measure heat-free characteristics of high power devices, and to get an in depth understanding of heat dissipation mechanisms, allowing one to build models that integrates thermal effects.

A. RF Power Characterization System

Fig. 1 shows a schematic of a novel characterization system that allows one to measure intermodulation distortion (IMD) products under pulse mode of operation at various load and source impedance terminations. It combines an improved pulsed load-pull system [6-7] and time-gated capabilities of a microwave spectrum analyzer. This system enables one to measure the device RF power performance under high power condition without self-heating effects. AlGaN/GaN HEMTs, grown on a SiC substrate, having a total gate width (W_G) of 250μm were studied. They exhibit an f_T of 22GHz, a breakdown voltage between 60 and 80V, and a current density of 800mA/mm. A negative slope is present in $I_{DS}(V_{DS})$ curves under high bias conditions typical of self-heating effects. RF power measurements are performed at 10GHz (V_{DS}=30V and V_{GS}=-0.5V) under continuous mode of operation (I_{DS}=125mA), and under pulsed regime (I_{DS}=144mA) using a pulse width of 5μs and a duty-cycle of 1.6%. Load and source impedance are tuned for maximum output power at the 1dB compression point under each condition of operation. As shown in Fig.2, an improvement of 2dB of the transistor gain is reported under pulse mode of operation. Consequently, the power of the carrier and the power of the intermodulation distortion products increase. As a result the IIP3 remains about the same, and the OIP3 increases by 2dBm. Pulsed IMD measurements are also performed selecting a V_{GS} value that achieves the same drain current as measured under continuous regime. Results are similar and lead to a higher gain and an increase of OIP3 by 2.3dBm.

B. Self-Heating Effects on Device RF Performance

We present in this section noise, power and linearity performance of AlGaN/GaN HEMTs under continuous mode of operation at various gate-to-source bias conditions in order to observe the evolution of the device characteristics when switching from an isothermal environment to a self-heating regime. Drain-to-source voltage (V_{DS}) is fixed at 22V while the gate-to-source voltage (V_{GS}) is varied resulting in a DC power (P_{DC}) sweep from 0.5W to 3.5W.

Noise parameters are measured from 2 to 14GHz using an ATN/Agilent noise measurement system. As shown in Fig.3 the minimum noise figure (F_{MIN}) degrades with increasing frequency and P_{DC}. The extracted equivalent noise resistance (R_N) is more sensitive to P_{DC} than to the frequency of operation. Its value in the self-heating regime is twice its value under isothermal conditions of operation, making the device more sensitive to source impedance termination.

Power and linearity characteristics are extracted at 8GHz. Load and source impedance are tuned for maximum output power at the 1dB compression point for all bias conditions. Fig.4 shows power sweep results under high bias condition. A 4W/mm power density is achieved with 27% power added efficiency (PAE), and a gain of 12 dB.

Noise, power and linearity parameters and figures of merit at 8GHz with respect to bias is shown in Table 1. For comparative purposes, the 1dB compression point obtained under each bias condition is chosen for reference. OP_{1dB} represents output power of the fundamental frequency at the 1dB compression point. IIP3 is the input power of the third order intercept point obtained from intermodulation distortion (IMD) measurements.

In those measurement P_{DC} is increased by reducing the magnitude of V_{GS} while V_{DS} = 22V, resulting in biasing conditions further away from pinch-off. Gain, efficiency and noise performance degrade when increasing P_{DC} while output power and linearity improve.

C. Device Modeling

Large-signal models are necessary to accurately design circuits that will require the device to operate in nonlinear region. This is achieved by combining model of the device current characteristics, and model of the device small-signal characteristics over a wide bias range. A standard Hybrid-Pi topology is used to simulate the small-signal characteristics of an AlGaN/GaN HEMT (Gate Width = 125×2μm, L_{GS} = 0.1μm, and L_{GD} = 3μm) from 1GHz to

15GHz over a complete range of bias conditions and temperatures. As shown in the equivalent circuit (Fig.5) the value of 15 parameters are determined to simulate the device characteristics under small-signal operations. The elements outside the dotted box represent the extrinsic part of the device. They come from the metal traces and the probing pads [10]. "ColdFET" measurements in conjunction with an improved equivalent circuit based on geometrical considerations of the device lead to the parasitic element values determination. Intrinsic element values are determined analytically from the intrinsic Y-parameters. Finally a CAD tool is used to optimize all parameters values. Small-signal simulations are performed from 1GHz to 15GHz at V_{GS} = -1 V and V_{DS} = 30 V at T = 150K (Fig.6), and at T = 300K. Table 2 summarizes the intrinsic element values at both temperatures. IV characteristics are modeled using a set of modified current expression, in order to fit the particularities of the considered power AlGaN/GaN HEMTs (Fig.7).

III. Reliability

Fabrication and thermal management are issues closely related to the reliability of GaN technology since they affect the lifetime, and the characteristics stability over time, of the devices.

A. Floating-Body Effects

One of the major substrate used to grow AlGaN/GaN HEMTs is SiC. In a wurtzite crystal structure, the lateral lattice constant of AlN (a = 3.11A) is an intermediate between the one of SiC (a = 3.086A) and the one of GaN (a = 3.189A). Therefore, in order to reduce the stress due to lattice mismatch [11-13], and to improve performance and reliability of the devices, an AlN sub-buffer layer is sometime grown between the SiC substrate and the GaN buffer layer. Also, AlN exhibits a high thermal conductivity (σ = 2W/cm-K); so its addition does not degrade heat transfer under high voltage operation. Such devices are measured under static conditions, and a kink in the I-V characteristics is reported. The body of the HEMT is formed on an AlN layer. Details of this type of structure are discussed in [13]. At 300K, the bandgap of AlN is 6.2ev, its high frequency dielectric constant is $\varepsilon_r^{AlN} = 4.77 \cdot \varepsilon_0$ [14], and its resistivity, ρ^{AlN}, is greater than $10^{14}\Omega.cm^{-1}$. These semiconductor properties suggest that the body of those devices is formed on a reasonably good insulator. Since no contacts are fabricated

between the body and the source, some properties similar to thin-film silicon on insulator (SOI) ($\varepsilon_r^{SiO_2} = 2.4 \cdot \varepsilon_0$, $\rho^{SiO_2} > 10^{14}\,\Omega.cm^{-1}$) can be expected [15-19]. When no contacts are fabricated between the body and the source, a kink is present in the current characteristics due to the existence of a body-to-source voltage V_{BS} that modifies the threshold voltage V_{TH} [15]. In addition, pulsed IV measurements are performed and results still exhibit a current kink ruling out the possibility of traps being the origin of this perturbance. Based on these observations, we consider the body of the devices grown on an AlN layer as floating. A method derived from SOI techniques is applied to extract the off-state floating body (FB) voltage (V_{BS}). The coherence of the results obtained confirms that FB effects are effectively present in this type of devices (Fig.8). Also, good agreement between the measured and modeled S-parameters over the entire drain bias range confirms validity of the T-circuit used to model the devices suffering from floating-body effect, and therefore, the validity of the floating–body assumption.

B. Thermal Analysis

A 2 finger GaN FET grown on SiC substrate is modeled as a stack of GaN, (active region = 4μm), SiC (substrate = 13mil), AuSn (solder = 1mil), and CuMoCu (base = 80mil) for thermal analysis purposes. The temperature of the base plate is fixed at 20°C, and simulations are performed under pulsed and continuous condition with a power density to dissipate of 5W/mm. Fig. 9 shows the peak GaN surface, the GaN/SiC interface and the CuMoCu surface temperatures for a series of 5ms pulses at 25% duty cycle. Timing parameters correspond to those that might be used in pulsed radar applications. A 30°C temperature drop in the thin GaN epi layer is reported, and the peak temperature is about 20°C lower than the continuous wave case (T_{CW} = 96°C). A temperature of the GaN layer of 300°C has been reported when grown on a sapphire substrate (σ = 0.28W/cm-K) with a base temperature fixed at 30°C [20]. The thermal conductivity of SiC (σ = 3.9W/cm-K) is 14 times higher and results in lower temperature.

IV. Circuit and System Applications

GaN-based transistors offer high power capabilities at high frequencies, and a reduce device size. Both military and commercial applications can benefit from these advantages.

A. Radar Applications

In active phased array radars (APAR), the transceivers (T/R) are placed between a radiating element and a phased shifter. This configuration reduces the power requirements of the power amplifier (PA) resulting in the possibility of using solid-state T/R modules. Until recently the PAs used in the transceiver of X-band radars (battle field range, air defense, missile guidance, and traffic control) were based on GaAs MESFETs technology; they roughly achieved a 5W output power, a 50% efficiency, and a 10dB gain for narrowband designs, and a 3W output power, a 30% efficiency and a gain of 11dB for broadband chipsets [21]. As seen in Equ.1, an improvement in output power results in an improvement of the radar detection range.

$$R_2 = R_1 \times \sqrt{\frac{ERP_2}{ERP_1}} \qquad (1)$$

$$ERP = P_T + G_A \qquad (2)$$

R is the detection range associated to the effective radiated power by the radar (ERP, in Watts), P_T is the transmitted power (dBm), and G_A is the antenna gain (dBi). Power densities up to 9W/mm at operating frequencies between 8 and 12GHz have been reported for AlGaN/GaN HEMTs, making the GaN technology very attractive.

B. Digital Communication Systems

The move to digital modulation provides more information capacity, higher data security, better quality telecommunications, and quicker system availability than analog modulation schemes. However, reducing the spectrum used to convey a certain amount of information results in more complex hardware, on both transmitter and receiver side. Another layer of complexity in many systems is multiplexing. It is used to separate different users of the spectrum. The principle types are FDMA (Frequency Division Multiple Access), TDMA (Time division Multiple Access), CDMA (Code Division Multiple Access). Most communication systems combine different forms of multiplexing. W-CDMA (Wideband CDMA) is one the popular air interface technologies for the 3rd generation (3G) RF cellular communications systems. It uses correlative codes to distinguish one user from another and FDMA.

A major trade-off in today's technologies used to build digital communication systems are the device output power and linearity. In order to meet the communication standards requirement in term of linearity, the devices are driven before compression reducing the output

power. Because of their high power capabilities, AlGaN/GaN HEMTs can achieve high output power and still operate before compression. This allows one to meet standards requirements while reducing the circuit complexity. Fig. 10 shows a snapshot of the spectrum at the output of a 2-finger device ($W_G = 250\mu m$) with a 3GHz input signal meeting the W-CDMA standard. The device is biased in class A operation, the 9dBm input power level of the signal drives it before compression, and the device output power under single tone stimulus is 28dBm. Under digital modulation, for similar bias condition and transmitted power, the power level transmitted in the adjacent channel is 30dB lower than the power level of the main channel. This results in an adjacent channel power ratio (ACPR) better than –40dB.

V. Conclusion

A complete investigation of GaN-based wide-bandgap electronic devices and circuits has been presented. It includes the understanding of the device technology (e.g. characterization systems, testing, and modeling), of the devices' reliability (e.g. fabrication, thermal effects), and the development of circuits and system applications. Such study is crucial provide a mature technology based on GaN.

Acknowledgment

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FIGURES

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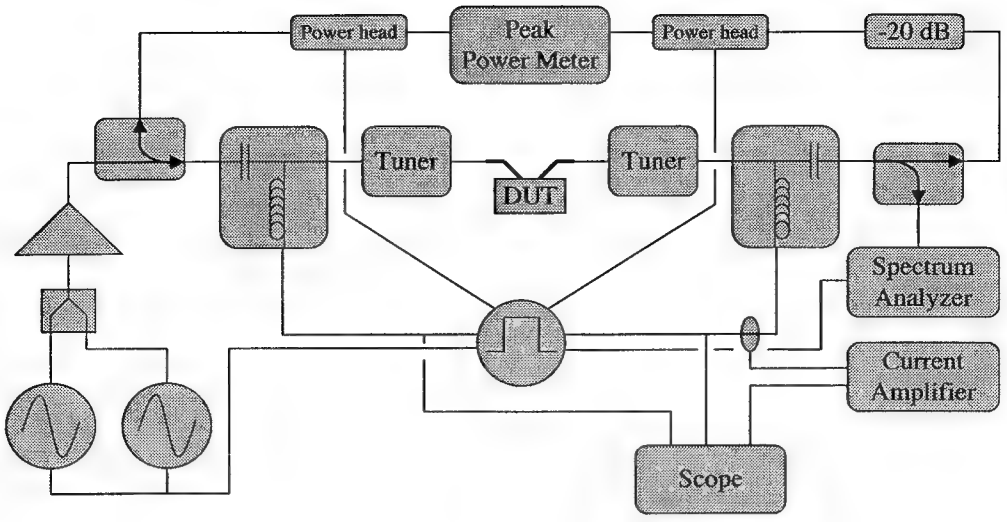


Figure 1

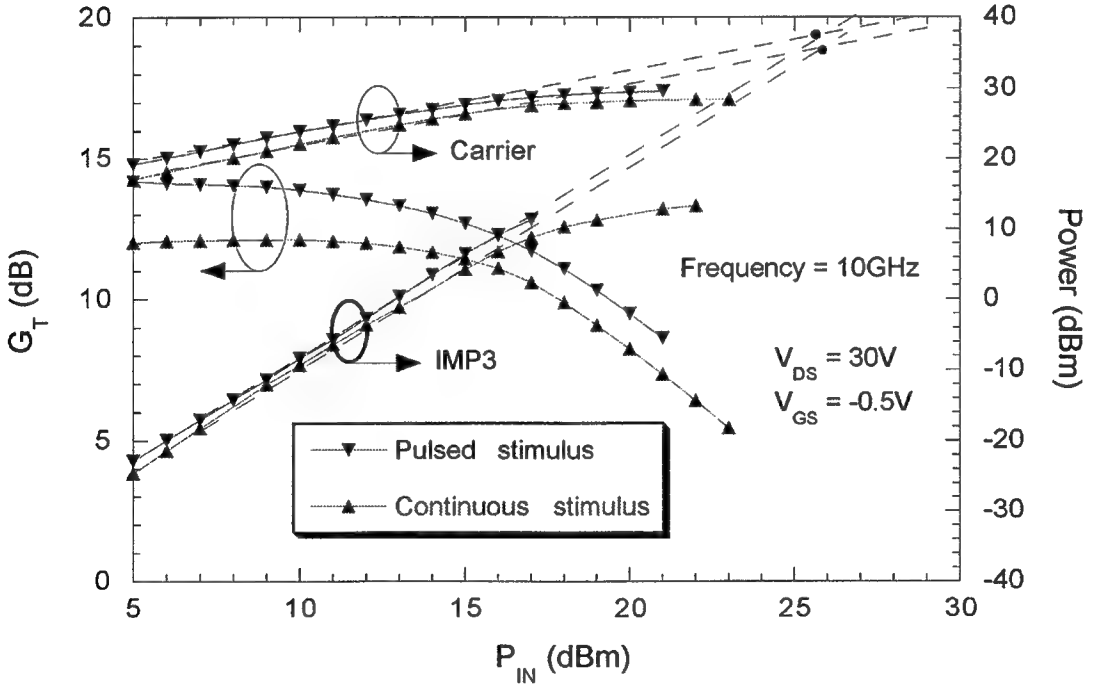
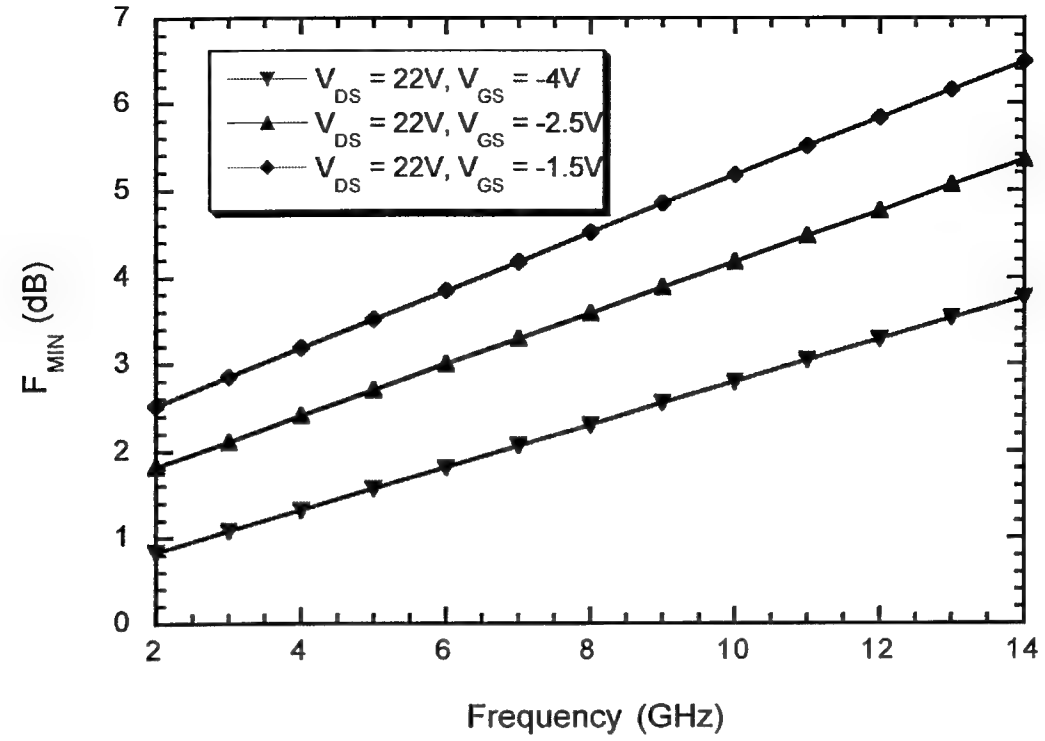


Figure 2



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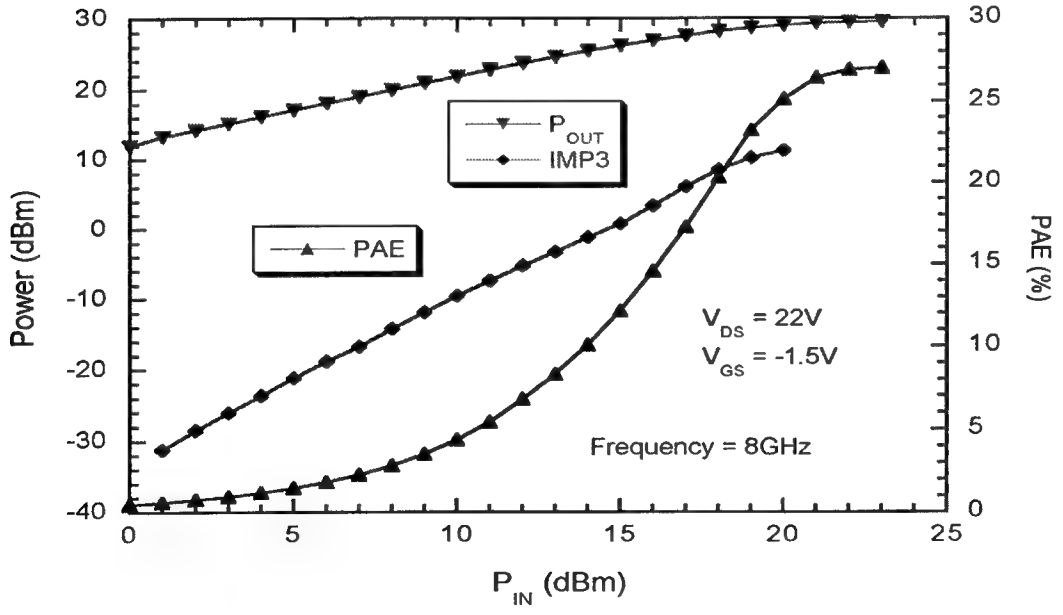


Figure 4

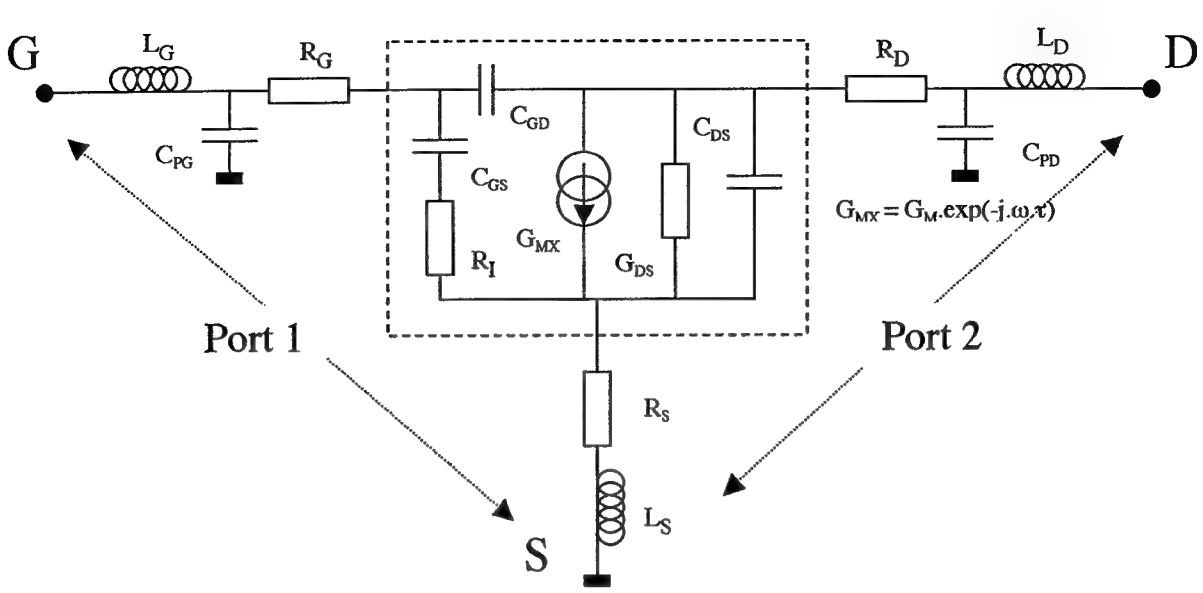
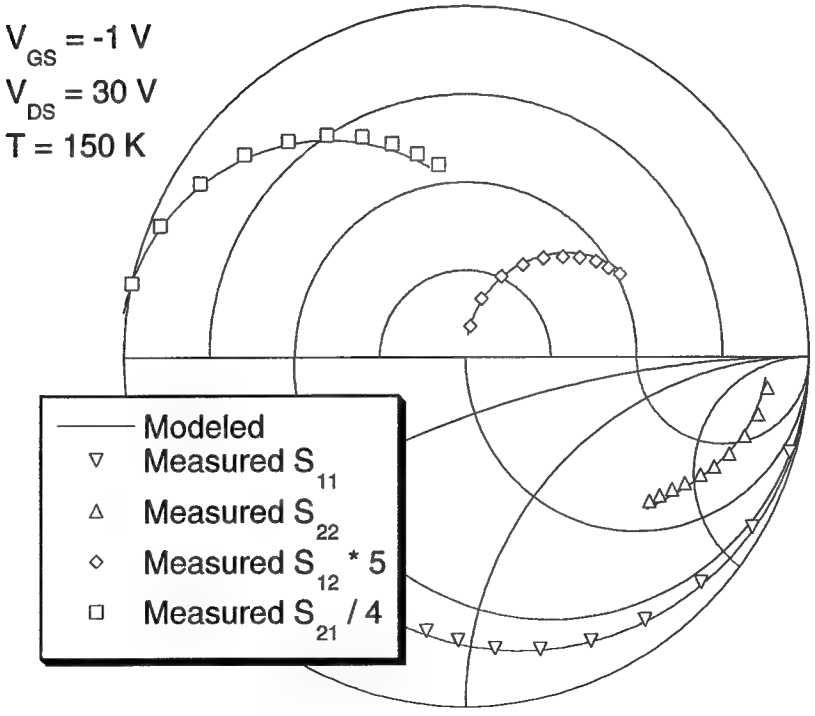


Figure 5



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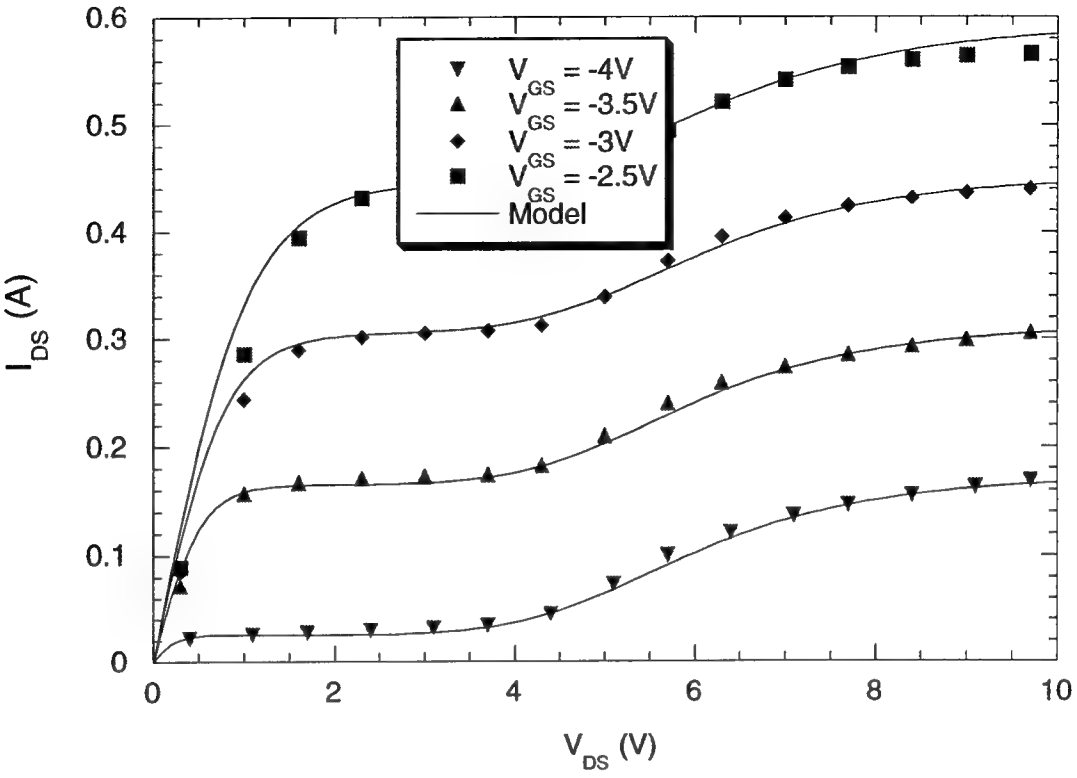

Figure 7

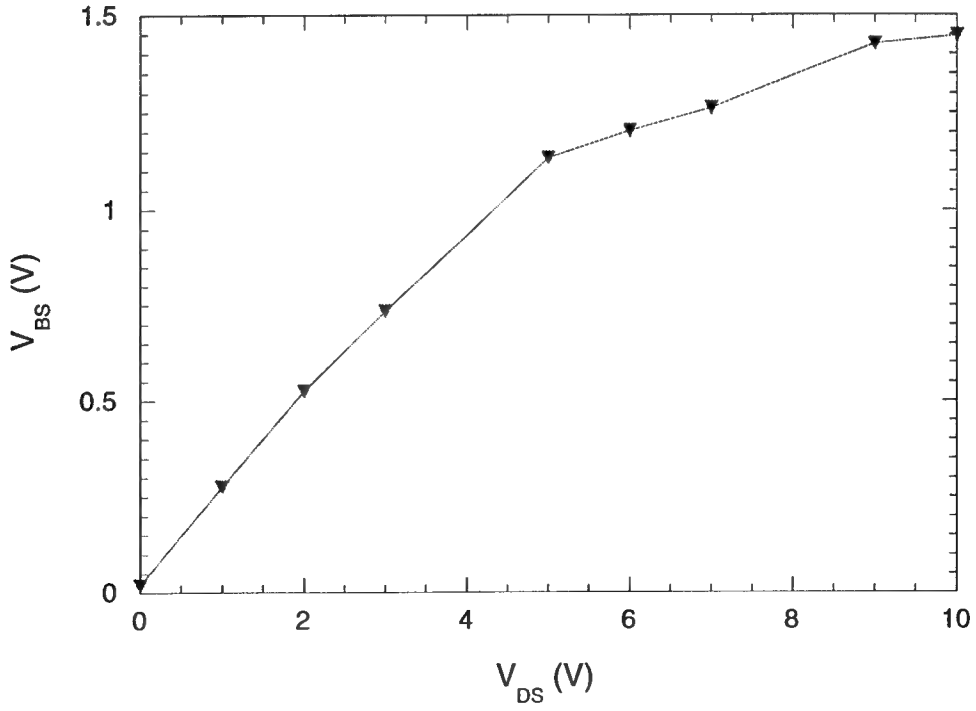

Figure 8

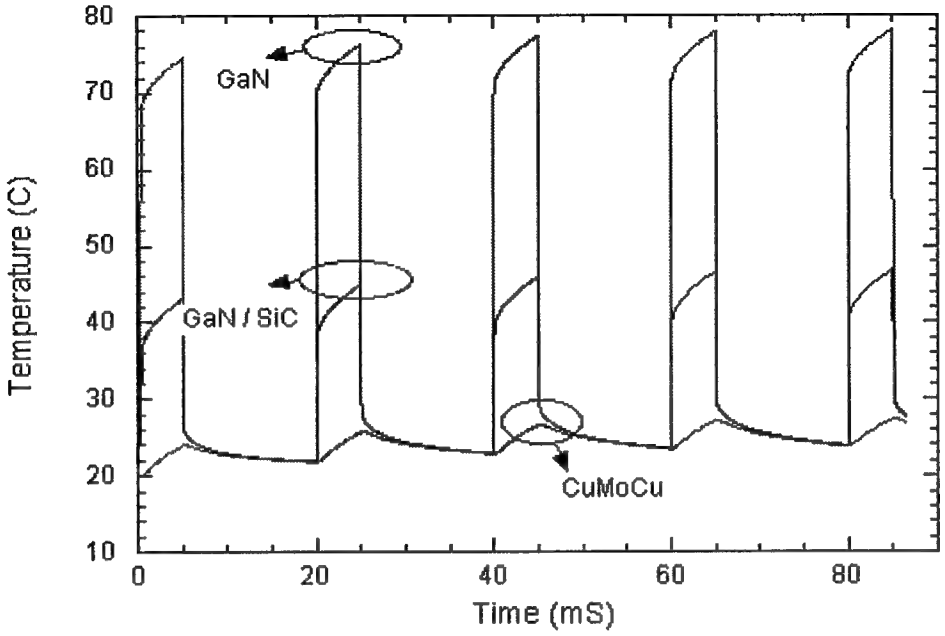

Figure 9

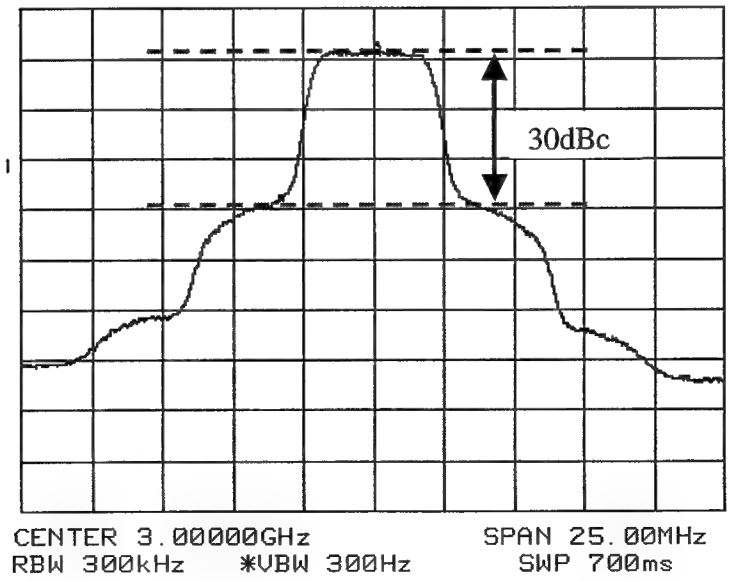

Figure 10

	V_{DS} = 22V V_{GS}= -1.5V	V_{DS} = 22V V_{GS}= -2.5V	V_{DS} = 22V V_{GS}= -4V
P_{DC} (W)	3.3	2.2	1
F_{MIN} (dB)	4.5	3.6	2.3
R_N (Ω)	57.6	45	27.9
Gain (dB)	12	13	14.5
OP_{1dB} (dBm)	26.9	25.9	25.5
PAE_{1dB} (%)	14.56	17.18	26
IIP3 (dBm)	24	23	20

Table 1

	C_{GS}	C_{DS}	C_{GD}	R_I	$1/G_{DS}$	G_M
T = 150K	210 fF	11 fF	21.5 fF	0.1 Ω	588 Ω	57 mS
T = 300K	182 fF	3.5 fF	26 fF	10 Ω	650 Ω	50 mS

Table 2

RF Performance And Thermal Analysis of AlGaN/GaN Power HEMTs in Presence of Self-Heating Effects

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Abstract - **Power, linearity and noise performance of AlGaN/GaN power HEMTs are measured at different gate-to-source bias condition in order to study the influence of self-heating on device RF performance. Additionally, a load-pull system, capable of measuring intermodulation distortion products under pulsed mode of operation, is implemented for the first time. This new system is used to investigate the impact of self-heating on power devices' linearity. Also, for the first time, the effect of the RF drive on thermal effects and power added efficiency (PAE) is investigated. This forms the basis of more accurate nonlinear models. Finally, thermal simulations of 2-finger GaN FETs are performed under pulsed and continuous regime to determine the temperature distribution caused by a 5W/mm power dissipation density.**

I. Introduction

Power amplifiers, that operate at microwave frequencies, are key elements for applications like phased array radar and base stations. AlGaN/GaN high electron mobility transistors (HEMTs) offer important advantages for high power applications due to the GaN wide bandgap [1-5]. GaN-based FETs offer power densities in the few W/mm range, cutoff frequencies (f_T) above 20GHz, and maximum frequency of oscillation (f_{MAX}) beyond 25 GHz. High power microwave circuits have already been proposed showing the great potential of this technology [6-8].

However, the overall power present in GaN-based power FETs is large and cannot be completely dissipated throughout the substrate. As a consequence AlGaN/GaN HEMTs suffer from self-heating effects. These effects perturb measurement results and reduce the lifetime of the devices under continuous mode of operation. The study of issues, like the reliability of GaN-based devices [9-10], and the understanding of heat dissipation in those transistors [11-12], is still in its early stages, and is crucial to providing a stable technology.

Operating devices during a short period of time permits one to control the heat dissipation in a device. Based on this assessment, pulsed-IV, pulsed S-parameter, and pulsed load-pull systems [11,12,13,14] have been implemented in order to measure heat-free characteristics of high power devices, and to get an in depth understanding of heat dissipation mechanisms, allowing one to build models that integrates thermal effects.

We investigate in Section II the changes of device characteristics under continuous mode of operation when switching from an isothermal environment to a heat regime in order to get a better understanding of self-heating effects on the device microwave performance. In Section III, an innovative load-pull system capable of measuring intermodulation distortion product under pulse mode of operation, is used to study the influence of self-heating on the device linearity. Section IV presents a method to relate thermal effects and PAE. Finally, Section V shows results of thermal simulation of GaN FETs on a SiC substrate, under pulsed and continuous stimulus.

II. Self-Heating Effects on Device RF Performance

AlGaN/GaN HEMTs, grown on a SiC substrate, having a total gate width (W_G) of 250μm were studied. They exhibit an f_T of 22GHz, a breakdown voltage between 60 and 80V, and a current density of 800mA/mm. A negative slope is present in $I_{DS}(V_{DS})$ curves under high bias conditions typical of self-heating effects.

We present in this section noise, power and linearity performance of those devices under continuous mode of operation at various gate-to-source bias conditions in order to observe the evolution of the device characteristics when switching from an isothermal environment to a self-heating regime. Drain-to-source voltage (V_{DS}) is fixed at 22V while the gate-to-source voltage (V_{GS}) is varied resulting in a DC power (P_{DC}) sweep from 0.5W to 3.5W.

Noise parameters were measured from 2 to 14GHz using an ATN/Agilent noise measurement system. As shown in Fig.1 the minimum noise figure (F_{MIN}) degrades with increasing frequency and P_{DC}.

The extracted equivalent noise resistance (R_N), presented in Fig.2, is more sensitive to P_{DC} than to the frequency of operation. Its value in the self-heating regime is twice its value under isothermal conditions of operation,

making the device more sensitive to source impedance termination.

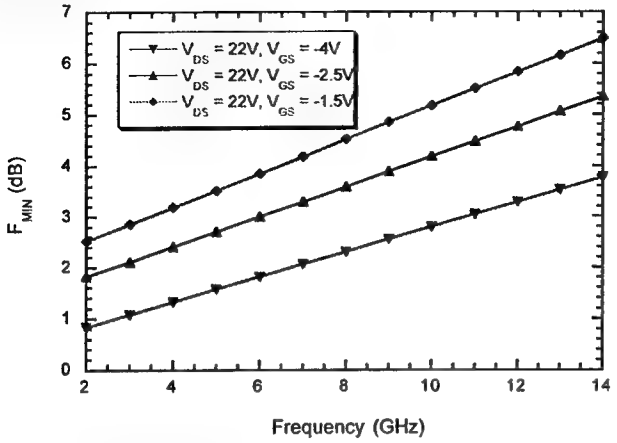

Fig. 1 Extracted minimum noise figure from low to high DC power versus frequency.

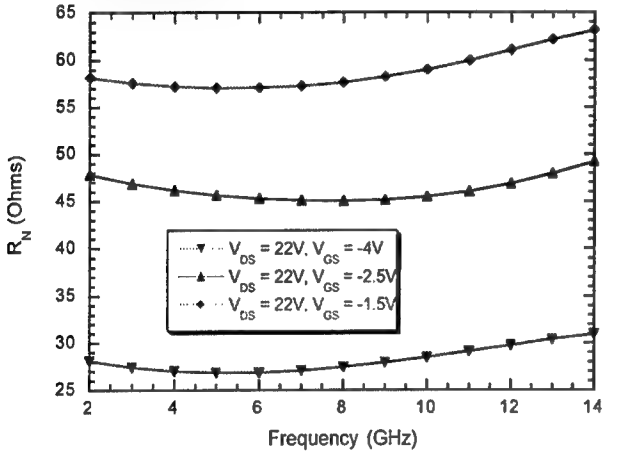

Fig. 2 Extracted equivalent noise resistance from low to high DC power versus frequency.

Power and linearity characteristics are extracted at 8GHz. Load and source impedance are tuned for maximum output power at the 1dB compression point for all bias conditions.

Fig.3 shows power sweep results under high bias condition. A 4W/mm power density is achieved with 27% power added efficiency (PAE), and a gain of 12 dB.

Noise, power and linearity parameters and figures of merit at 8GHz with respect to bias is shown in Table 1. For comparative purposes, the 1dB compression point obtained under each bias condition is chosen for reference.

OP_{1dB} represents output power of the fundamental frequency at the 1dB compression point. IIP3 is the input power of the third order intercept point obtained from intermodulation distortion (IMD) measurements.

In those measurement P_{DC} is increased by reducing the magnitude of V_{GS} while V_{DS} = 22V, resulting in biasing conditions further away from pinch-off. Gain, efficiency and noise performance degrade when increasing P_{DC} while output power and linearity improve.

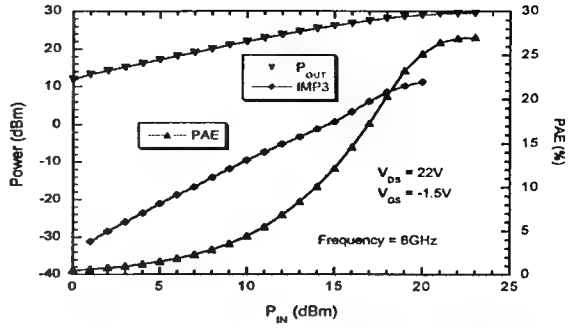

Fig. 3 Power results of an AlGaN/GaN HEMT with W_G=250µm at 8GHz, and at (V_{DS} = 22V; V_{GS} = 1.5V).

	V_{DS} = 22V V_{GS}= -1.5V	V_{DS} = 22V V_{GS}= -2.5V	V_{DS} = 22V V_{GS}= -4V
P_{DC} (W)	3.3	2.2	1
F_{MIN} (dB)	4.5	3.6	2.3
R_N (Ω)	57.6	45	27.9
Gain (dB)	12	13	14.5
OP_{1dB} (dBm)	26.9	25.9	25.5
PAE_{1dB} (%)	14.56	17.18	26
IIP3 (dBm)	24	23	20

Tab. 1 Comparative table of CW performance at 8GHz with respect to the bias condition (dissipated power).

III. Pulsed IMD Measurement System

We present in this section a novel characterization system that allows one to measure intermodulation distortion products under pulse mode of operation. It combines an improved pulsed load-pull system [11-12] and time-gated capabilities of a microwave spectrum analyzer. This system enables one to measure device linearity under high power condition without self-heating effects. Fig.4 shows a schematic of the setup.

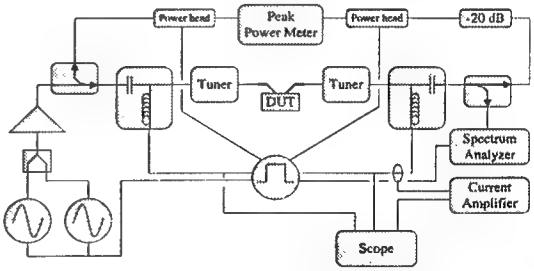

Fig. 4 Schematic of the pulsed load-pull/Intermodulation distortion measurement system.

IMD measurements are performed at 10GHz (V_{DS}=30V and V_{GS}=-0.5V) under continuous mode of operation (I_{DS}#125mA), and under pulsed regime (I_{DS}#144mA) using a pulse width of 5µs and a duty-cycle of 1.6%. Load and source impedance are tuned for maximum output power at the 1dB compression point under each condition of operation.

As shown in Fig.5, an improvement of 2dB of the transistor gain is reported under pulse mode of operation. Consequently, the power of the carrier and the power of

the intermodulation distortion products increase. As a result the IIP3 remains about the same, and the OIP3 increases by 2dBm.

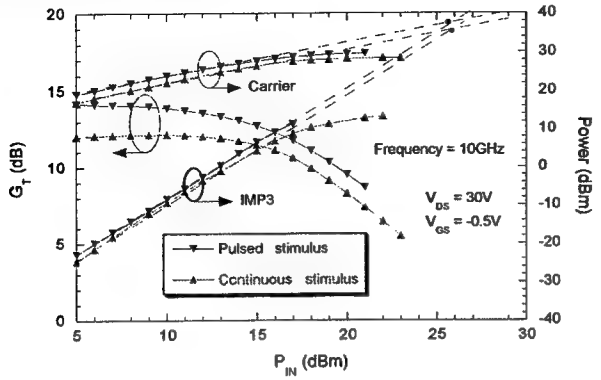

Fig. 5 Pulsed IMD measurement results.

Pulsed IMD measurements are also performed selecting a V_{GS} value that achieves the same drain current as measured under continuous regime. Results are similar and lead to a higher gain and an increase of OIP3 by 2.3dBm.

IV. Self-Heating Effects on PAE

When the total power (P_T) present in a device exceeds its power dissipation capabilities, represented by the power threshold P_{THRES}, the device suffers from thermal effects. The excess of power (ΔP) results in an increase of the device temperature modifying the carrier electronic transport properties and therefore changes the device characteristics [15].

In this section we relate the changes in ΔP caused by an RF drive and the PAE of a device suffering from self-heating effects.

A. Power Threshold

The value of P_{THRES} is determined on a 250μm device using temperature dependent DC-IV measurement results. As reported in [11] the drain voltage threshold where the drain current characteristics degrade increases when decreasing temperature of operation. This allows an accurate determination of the threshold value. Measuring the power threshold at various low temperatures enables accurate extrapolation of P_{THRES} at room temperature.

As shown in Fig.6, a 0.84W/mm P_{THRES} is extracted at 293K.

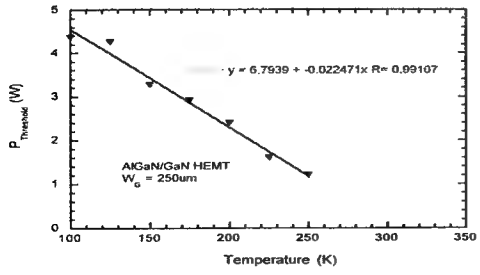

Fig. 6 Extraction of P_{THRES} at 293K.

B. DC Case

The drain current characteristics of a transistor can be expressed at a given bias point with the admittance Y:

$$I_{DS} = Y \cdot V_{DS} \qquad (1)$$

Without an RF drive, the total power present in a device, P_T, can be expressed by:

$$P_T = P_{DC} \approx V_{DS} \cdot I_{DS} \qquad (2)$$

Fig.7 illustrates the variation of the drain current I_{DS} and the variation of the admittance Y with P_T at a given V_{GS}, of a device suffering from self-heating.

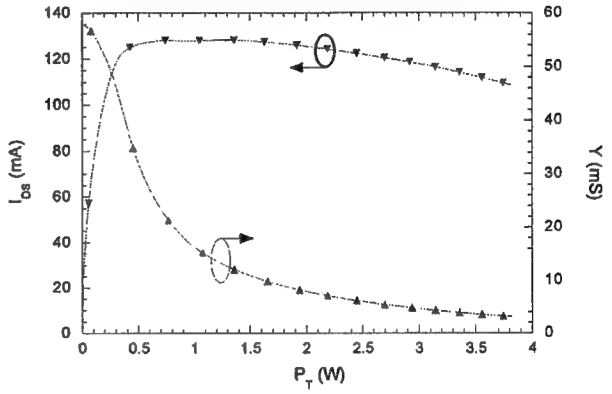

Fig. 7 Admittance Y and drain current I_{DS} versus total power P_T of a 250μm AlGaN/GaN device at fixed V_{GS}.

C. DC + RF Case

In presence of an RF drive P_T can be written as [15]:

$$P_T = P_{DC} + P_{IN}^{RF} - P_{OUT}^{RF} = P_{IN} \cdot (\eta PAE - 1) \cdot (G - 1) \qquad (3)$$

where P_{IN} is the power level of the RF drive, and G is the gain. The parameters in Eq.3 can be determined at any bias points and terminations from power measurements. Fig.8 shows a decrease in total power to dissipate in a 250um device when increasing the input power level, and causes a reduction of the thermal effect's magnitude. This results in an increase of the drain-to-source current.

The power added efficiency of a device increases with the input power level. In a class A operation the improvement in PAE starts to become significant when the device goes into compression as P_{DC} decreases while P_{out}-P_{in} increases. In presence of thermal effect, the reduction of P_T causes I_{DS} to increase working against the negative dc component resulting from the harmonics generated by the devices' non-linearity. As a consequence, in presence of thermal effects, the peak PAE is not as high as in a heat free device.

Integration of the thermal effect magnitude changes with the input of the RF drive in nonlinear model would lead to more accurate prediction of the device behavior.

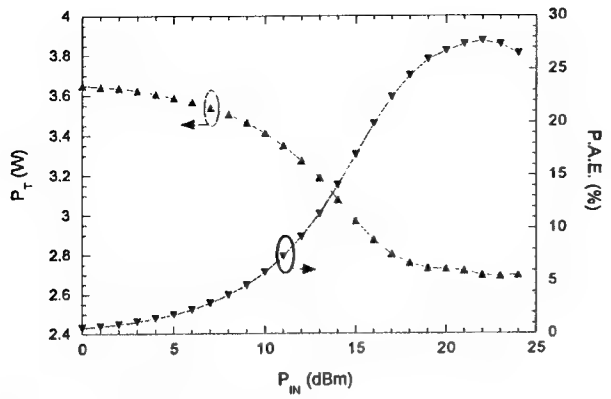

Fig. 8 P_T and PAE versus P_{IN}.

V. Temperature Analysis

A 2 finger GaN FET grown on SiC substrate is modeled as a stack of GaN, (active region = 4μm), SiC (substrate = 13mil), AuSn (solder = 1mil), and CuMoCu (base = 80mil) for thermal analysis purposes. The temperature of the base plate is fixed at 20°C, and simulations are performed under pulsed and continuous condition with a power density to dissipate of 5W/mm.

Fig. 8 shows the peak GaN surface, the GaN/SiC interface and the CuMoCu surface temperatures for a series of 5ms pulses at 25% duty cycle. Timing parameters correspond to those that might be used in pulsed radar applications. A 30°C temperature drop in the thin GaN epi layer is reported, and the peak temperature is about 20°C lower than the continuous wave case (T_{CW} = 96°C).

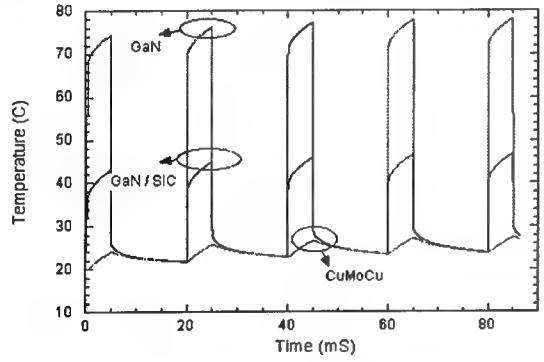

Fig.8 Temperature response at the surface of the GaN layer, at the GaN / SiC interface, and at the CuMoCu surface, under pulsed stimulus.

A temperature of the GaN layer of 300°C has been reported when grown on a sapphire substrate (σ = 0.28W/cm-K) with a base temperature fixed at 30°C [16]. The thermal conductivity of SiC (σ = 3.9W/cm-K) is 14 times higher and results in lower temperature.

VI. Conclusion

Power, noise and linearity measurements have been carried out on-wafer under various power conditions to investigate self-heating effects on AlGaN/GaN power devices. In addition, measurement results using an innovative pulsed IMD system give an in depth understanding of the influence of self-heating on the RF device performance. Also, the influence of thermal effects on the PAE is investigated. Finally, the temperature distribution in GaN FETs under large power density is presented. This study allows one to build more accurate nonlinear models of devices exhibiting thermal effects.

Acknowledgement

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MEASUREMENTS AND MODELING OF FLOATING-BODY EFFECTS IN ALGAN/GAN POWER HEMTS

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Keywords : Microwave Power FETs, GaN HEMTs, Floating-Body Effects, Modeling.

ABSTRACT

AlGaN/GaN power HEMTs, grown on an AlN sub-buffer layer to reduce lattice mismatch between the SiC substrate and the GaN buffer layer, are measured under static conditions, and a kink in the I-V characteristics is reported. In general, if the GaN buffer layer is insulating and substrate conduction is avoided, then kinks in the I-V characteristics appear. Various experiments are performed and suggest this kink is associated with floating-body effects. A method to extract the off-state body-to-source voltage (V_{BS}) is applied to those devices. In addition, a model of the current characteristics where floating-body effects are predominant is proposed. The model is based on extraction and modeling of the bias-dependent threshold voltage (V_{TH}). This forms the basis for accurate large-signal models that include floating-body effects. To our knowledge, this is the first time that floating-body effects are reported and modeled in GaN-based FETs.

I- INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMTs) offer important advantages for high power applications due to the GaN wide bandgap [1-5]. High power microwave circuits have already been proposed showing the great potential of this technology [6-8]. However, the study of issues, like the reliability of GaN-based devices [9-10], and the understanding of heat dissipation in those transistors [11], is still in its early stages.

In a wurtzite crystal structure, the lateral lattice constant of AlN (a = 3.11A) is an intermediate between the one of SiC (a = 3.086A) and the one of GaN (a = 3.189A). Therefore, in order to reduce the stress due to lattice mismatch [12-14], and to improve performance and reliability of devices, an AlN sub-buffer layer is grown between the SiC substrate and the GaN

buffer layer. Also, AlN exhibits a high thermal conductivity (σ = 2W/cm-K); so its addition does not degrade heat transfer under high voltage operation.

In this paper, we report the study of GaN-based FETs grown on a SiC substrate using an AlN sub-buffer layer. We will first demonstrate that floating-body effects in these devices cannot be neglected. Based on this assumption, a method is used to extract the off-state Floating-Body (FB) voltage of these AlGaN/GaN HEMTs. Finally, an empirical model is proposed to take into account these effects in the current characteristics.

II- Evidence Of Floating-Body Effects

Fig.1 illustrates a cross-section of AlGaN/GaN HEMTs that exhibit this effect. The body of the HEMT is formed on an AlN layer. Details of this type of structure are discussed in [14]. At 300K, the bandgap of AlN is 6.2ev, its high frequency dielectric constant is $\varepsilon_r^{AlN} = 4.77 \cdot \varepsilon_0$ [15], and its resistivity, ρ^{AlN}, is greater than $10^{14}\Omega.cm^{-1}$. These semiconductor properties suggest that the body of those devices is formed on a reasonably good insulator. Since no contacts are fabricated between the body and the source, some properties similar to thin-film SOI ($\varepsilon_r^{SiO_2} = 2.4 \cdot \varepsilon_0$, $\rho^{SiO_2} > 10^{14}\,\Omega.cm^{-1}$) can be expected [16-20].

When no contacts are fabricated between the body and the source, a kink is present in the current characteristics due to the existence of a body-to-source voltage V_{BS} that modifies the threshold voltage V_{TH} [16].

As shown in Fig.2, a kink is observed in the current characteristics of these HEMTs. This kink has already been measured in similar AlGaN/GaN devices [9, 21] but has not been studied. When trapping effects are dominant, adding a delay between each drain voltage sweep gives time for trapped carriers to relax, and current characteristics become kink-free. In those devices, even a delay of 120 seconds does not yield to a kink-free characteristic (Fig.2). In addition, pulsed IV measurements are performed and results still exhibit a current kink ruling out the possibility of traps being the origin of this perturbance.

Based on these observations, we consider the body of those devices as floating. In Section III a method derived from SOI techniques is applied to extract the off-state FB voltage (V_{BS}). The coherence of the results obtained confirms that FB effects are effectively present in this type of devices.

In addition, IV characteristics have been measured on AlGaN/GaN devices with different layer structure. HEMTs, grown on sapphire with a GaN buffer (no AlN in structure), show kinks if the GaN buffer is insulating (a resistivity of $10^8\Omega.cm^{-1}$ has been measured on undoped GaN). If the nucleation process is off, buried charges are present in the buffer, presumably from polarization effects, and the kinks are not observed. Therefore, the floating-body assessment can be extended to other AlGaN/GaN HEMTs if the GaN buffer layer is insulating and substrate conduction is avoided.

III- Extraction Of The Off-State Body-To-Source Voltage

A method to extract the off-state FB has been presented [22, 23]. C-V and S-parameter measurements along with an equivalent circuit were used to determine the FB voltage. We propose in this section to apply this technique to extract the off-state FB voltage of our AlGaN/GaN HEMTs.

When the gate bias (V_{GS}) is below the threshold voltage (V_{TH}) the channel resistance is large and the transistor can be represented with the T-circuit shown in Fig.3. The impedance parameters of this circuit are:

$$Z_{11} = R_G + R_S + \frac{1}{j\omega}\cdot\left[\frac{1}{C_{GB}} + \frac{1}{C_{SB}}\right]$$
$$Z_{12} = Z_{21} = R_S + \frac{1}{j\omega}\cdot\left[\frac{1}{C_{SB}}\right] \qquad [1]$$
$$Z_{22} = R_D + R_S + \frac{1}{j\omega}\cdot\left[\frac{1}{C_{DB}} + \frac{1}{C_{SB}}\right]$$

Where R_G, R_S, and R_D are the parasitic resistances associated with the gate, source, and drain. C_{SB} represents the source-body junction capacitance, C_{DB} the drain-body junction capacitance, and C_{GB} the gate-body capacitance.

Using Eq.1 along with a bias dependent S-parameter measurement system allows one to extract the capacitances values at various drain biases when $V_{GS} < V_{TH}$. Fig. 4 presents Z-parameter measurement results used for the extraction of the capacitances at one bias point.

Once the source-body junction capacitance is extracted, the FB voltage is determined using the PN junction capacitance model of [22-24]:

$$C_{SB}(V_{SB}) = \frac{C_{J0}}{\left(1+\frac{V_{SB}}{V_J}\right)^m} \qquad [2]$$

Where C_{j0} is the zero bias junction capacitance, V_J the junction built-in potential, m the junction grading coefficient, and V_{SB} the FB voltage. This expression can be rewritten as:

$$V_{SB} = V_J \cdot \left[\exp\left(\frac{\ln\left(\frac{C_{J0}}{C_{SB}}\right)}{m} \right) - 1 \right] \qquad [3]$$

Before using this relation parameters, V_J, C_{J0}, and m must be determined. As presented in [22, 23] the capacitance C_T that results from the series connection of C_{SB} and C_{DB} can be extracted from measured Z_{22}, and can also be approximated in a first order by:

$$C_T = \frac{1}{\frac{1}{C_{SB}} + \frac{1}{C_{DB}}} \approx \frac{C_{J0}}{1+\left(1+\frac{V_{DS}}{V_J}\right)^m} \qquad [4]$$

This expression can be rewritten as:

$$\frac{C_T}{C_{J0} - C_T} = \left(1+\frac{V_{DS}}{V_J}\right)^{-m} \qquad [5]$$

Fig. 5 illustrates the extraction of C_{J0}, V_J and m. Best fit analysis gives C_{J0} between 950fF and 1020fF, V_J = 1.85V and m = 0.08.

Fig. 6 and Fig. 7 respectively, show the extracted capacitances and the off-state FB voltage of the device.

Good agreement between the measured and modeled S-parameters (Fig.8) over the entire drain bias range confirms validity of the T-circuit used and, therefore, the validity of the floating–body assumption.

IV- Modeling Of IV-Characteristics

Modification of the threshold voltage (V_{TH}) [16] is one of the effects due to a floating body. Kink in the current characteristics of an AlGaN/GaN HEMT is modeled in this section by extracting and modeling V_{TH}.

A simple drain current characteristic can be modeled by:

$$I_{DS}^{basic} = g_0 \cdot \left(V_{GS} - V_{TH}^0\right) \cdot \tanh\left(\frac{V_{DS}}{\delta(V_{GS})}\right) \qquad [6]$$

Where g_0 is a parameter with the units of conductance, V_{TH}^0 the threshold voltage, V_{GS} the gate-to-source bias, V_{DS} the drain-to-source bias, and $\delta(V_{GS})$ is a linear relation that defines the knee of the current characteristics.

A drain current characteristic that exhibits a kink due to a bias-dependent threshold voltage can be expressed by:

$$I_{DS}^{measured} = g_0 \cdot \left(V_{GS} - V_{TH}(V_{DS}, V_{GS})\right) \cdot \tanh\left(\frac{V_{DS}}{\delta(V_{GS})}\right) \qquad [7]$$

g_0, $\delta(V_{GS})$, and V_{TH}^0 can be extracted by fitting the part of the IV characteristics where V_{DS} is small enough to consider constant the threshold voltage V_{TH}. This drain voltage range defines the part of the IV curves on the left side of the kink.

It is therefore possible to extract the varying threshold voltage using:

$$V_{TH}(V_{DS}, V_{GS}) = V_{TH}^0 - \frac{\Delta I_{DS}}{g_0 \cdot \tanh\left(\frac{V_{DS}}{\delta(V_{GS})}\right)} \qquad [8]$$

Where $\Delta I_{DS} = I_{DS}^{measured} - I_{DS}^{basic}$. Fig.9 shows the extracted threshold voltage versus the drain bias for various gate biases. V_{TH} has an asymmetrical step shape, and can be modeled with the expression:

$$V_{TH}(V_{DS}, V_{GS}) = V_{TH}^0 + \frac{\Delta V_{TH}}{1 + \exp\left(-\frac{V_{DS} - V_{kink}(V_{GS})}{\rho(V_{DS})}\right)} \qquad [9]$$

where ΔV_{TH} expresses the maximum variation of V_{TH}, V_{kink} determines the position of the step relative to the drain bias, and $\rho(V_{DS})$ controls how asymmetric the step is.

The variation of $V_{kink}(V_{GS})$ is similar to the variation of the drain voltage $V_{DS}^{max}(V_{GS})$ that maximizes (dI_{DS}/dV_{DS}). In Fig.10a and Fig.10b we observe that the kink starts at higher values of V_{DS} when increasing the gate bias. Finally V_{kink} is modeled using the expression:

$$V_{kink}(V_{GS}) = \alpha + V_{DS}^{max}(V_{GS}) = \alpha + A + B \cdot \exp\left(\frac{V_{GS} - C}{D}\right) \qquad [10]$$

Best fits were obtained for $\alpha = 1V$, $A = 4.95V$, $B = 0.8V$, $C = -2V$, $D = 0.8V$.

$\rho(V_{DS})$ is modeled using a linear relation. An optimization routine gives $\Delta V_{TH} = -0.55V$, and $\rho(V_{DS}) = 0.24 + 0.14*V_{DS}$. Fig.9 shows extracted and modeled data for the threshold voltage.

Finally the model of the threshold voltage is used to calculate the drain current using Eq.7. Measured and modeled data are presented in Fig.11. Simulated results agree well with the measured data over the bias range where floating-body effects are predominant. At higher gate voltage, the DC power density becomes too high and self-heating cannot be neglected.

V- CONCLUSION

Reliability is one of the many issues facing the design of AlGaN/GaN power devices. Use of an AlN sub-buffer layer improves this aspect but generates effects similar to the ones observed in SOI technology. Some of these effects are undesirable and it is important to understand them, and how they affect the device and circuit performance.

We report in this paper existence of floating-body effects in some type of AlGaN/GaN HEMTs. We extracted the off-state body-to-source voltage that is one of the parameters to consider in the presence of FB effects, and a current model that incorporates effects of this FB voltage is presented.

ACKNOWLEDGEMENT

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FIGURE CAPTIONS

FIG. 1: Layer structure of AlGaN/GaN HEMTs.

FIG. 2: IV characteristics of a GaN HEMT with AlN nucleation layer on SiC subatrate.

FIG. 3: Equivalent circuit for large value of channel resistance.

FIG. 4: Evolution of the inverse of the imaginary part of the Z-parameters at one bias condition for capacitances extraction.

FIG. 5: Plot of measured and modeled drain-source C-V data based on Equ.5 for extraction of parameters m and V_J.

FIG. 6: Extracted capacitances values versus drain voltage.

FIG. 7: Extracted off-state body-to-source voltage versus drain bias.

FIG. 8: Plot of measured and modeled S-parameter data.

FIG. 9: Plot of extracted and modeled threshold voltage V_{TH} versus drain voltage at various gate bias conditions.

FIG. 10A: Plot of the first derivative of drain current versus drain voltage at various gate bias conditions.

FIG. 10B: Plot of extracted and modeled V_{DS}^{MAX}.

FIG. 11: Plot of measured and modeled drain current characteristics.

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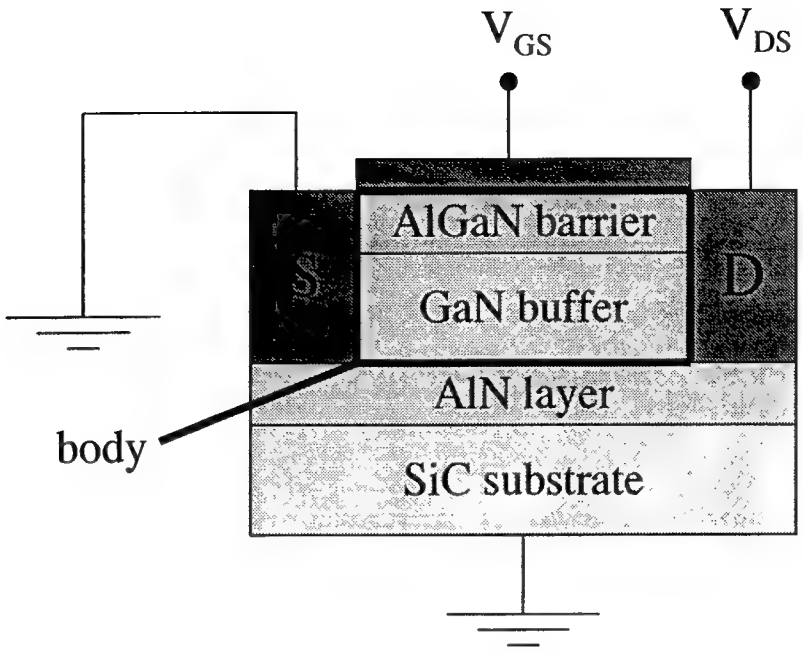

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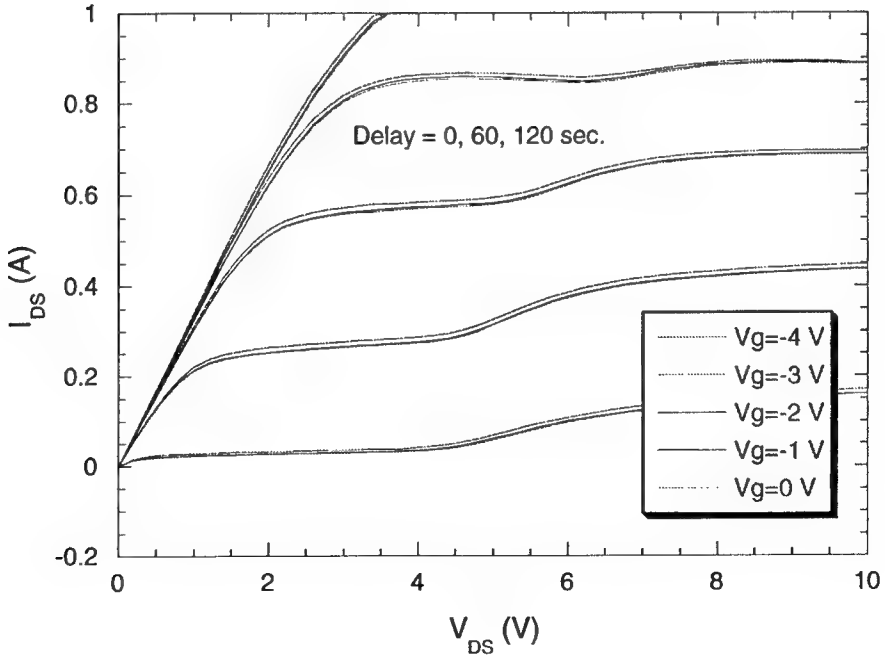

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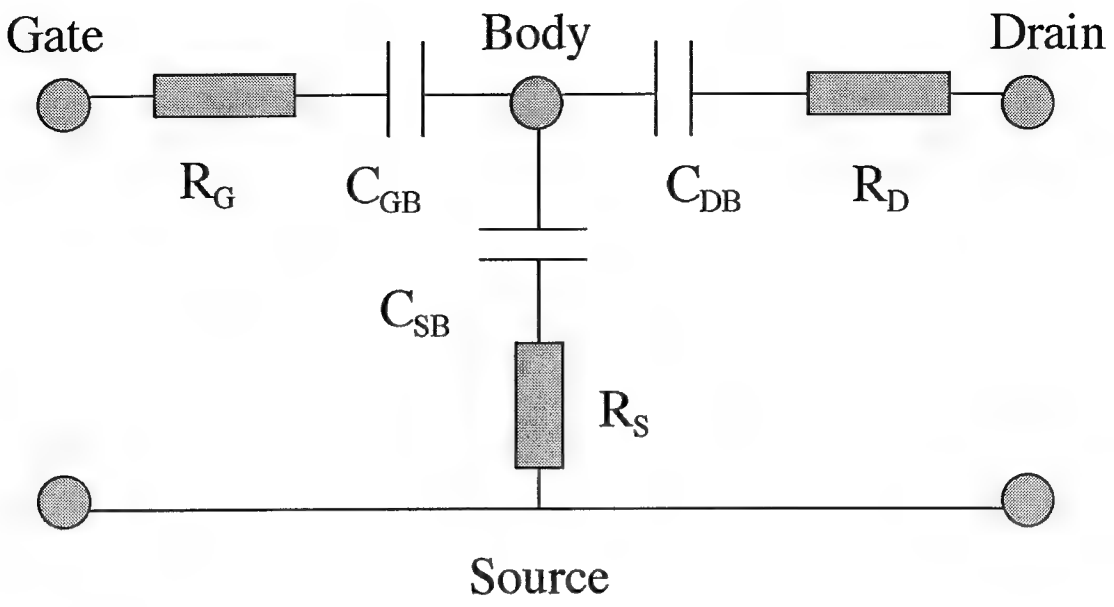

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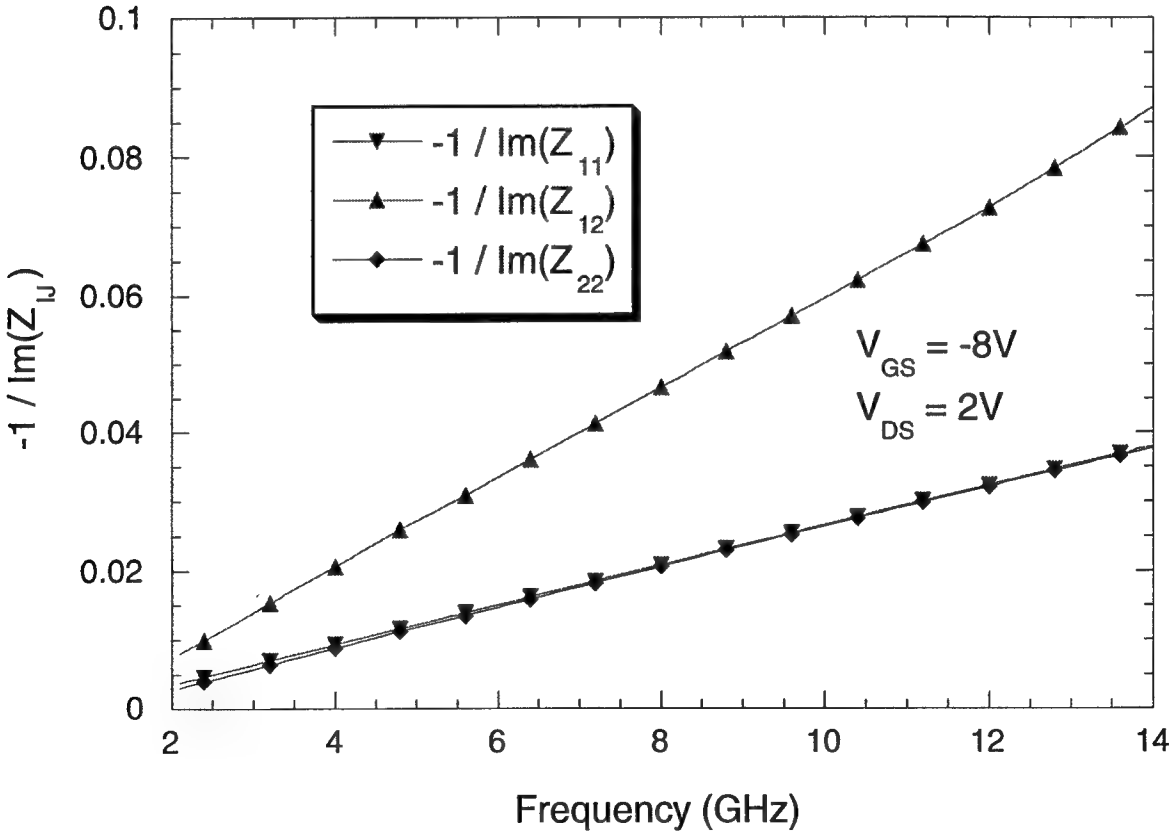

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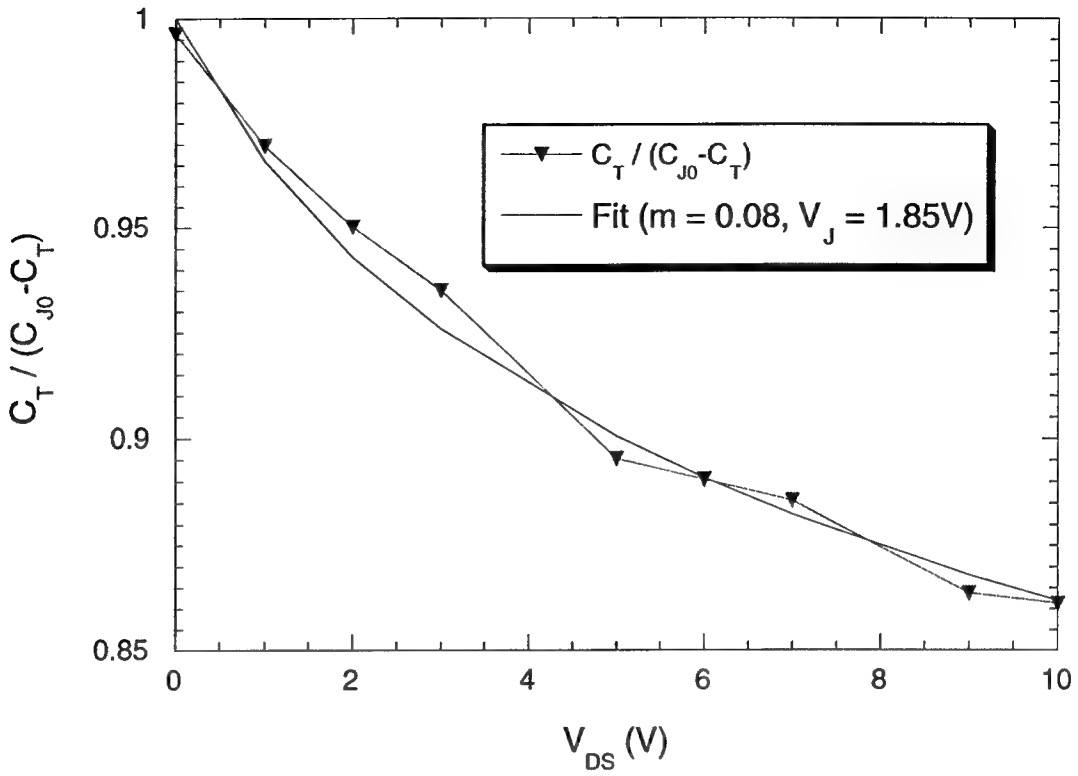
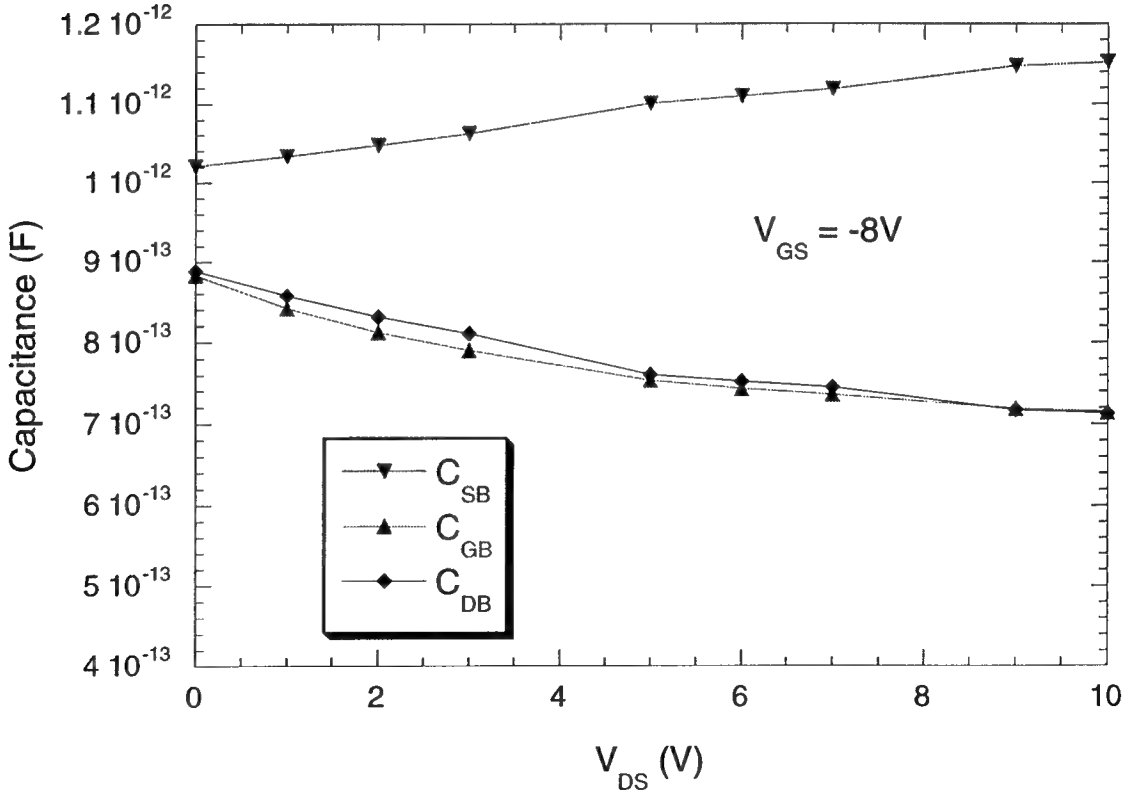


Figure 5



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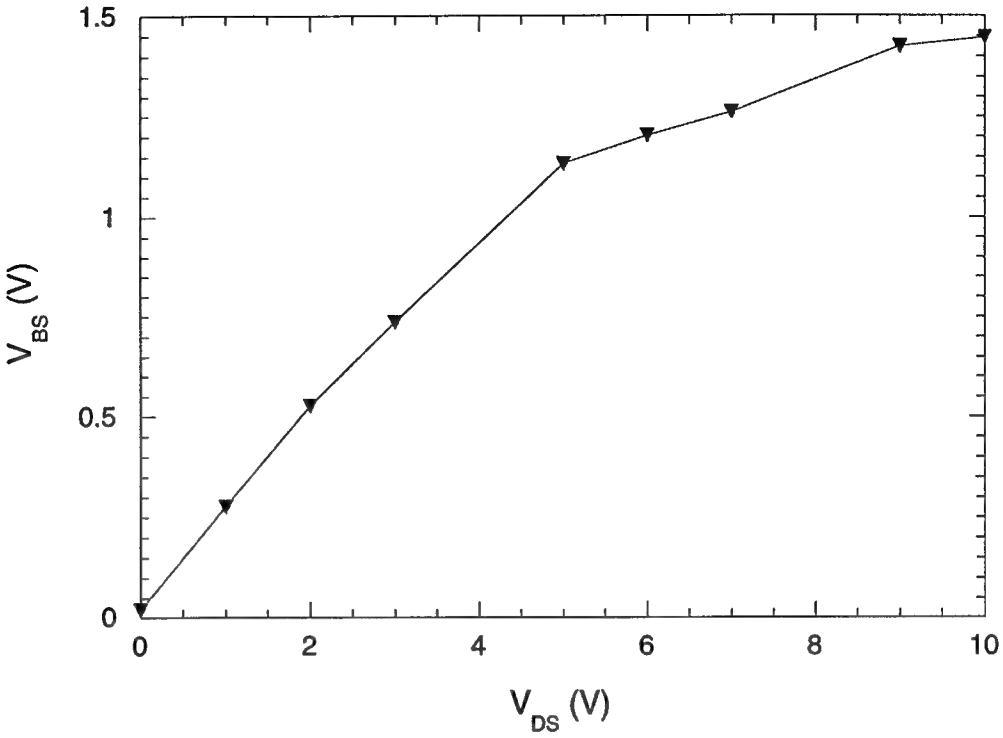

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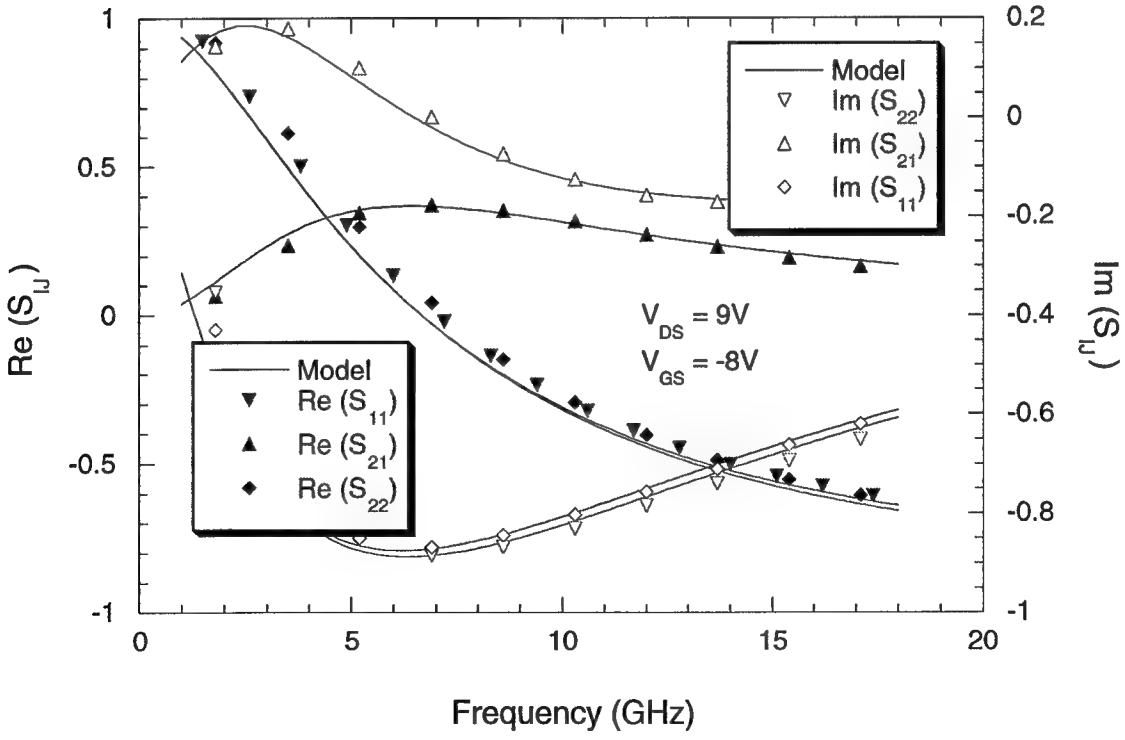

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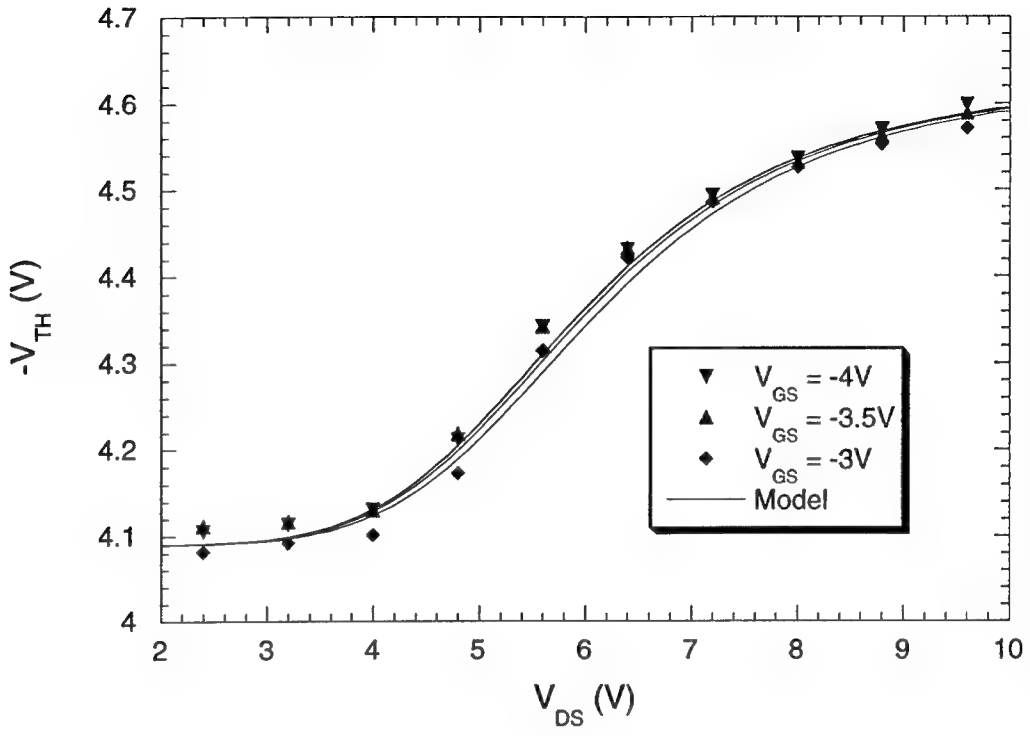

4.7
4.6
4.5
4.4
4.3
4.2
4.1
4
-V_TH (V)
2
3
4
5
6
7
8
9
10
V_DS (V)
V_GS = -4V
V_GS = -3.5V
V_GS = -3V
Model

Figure 9

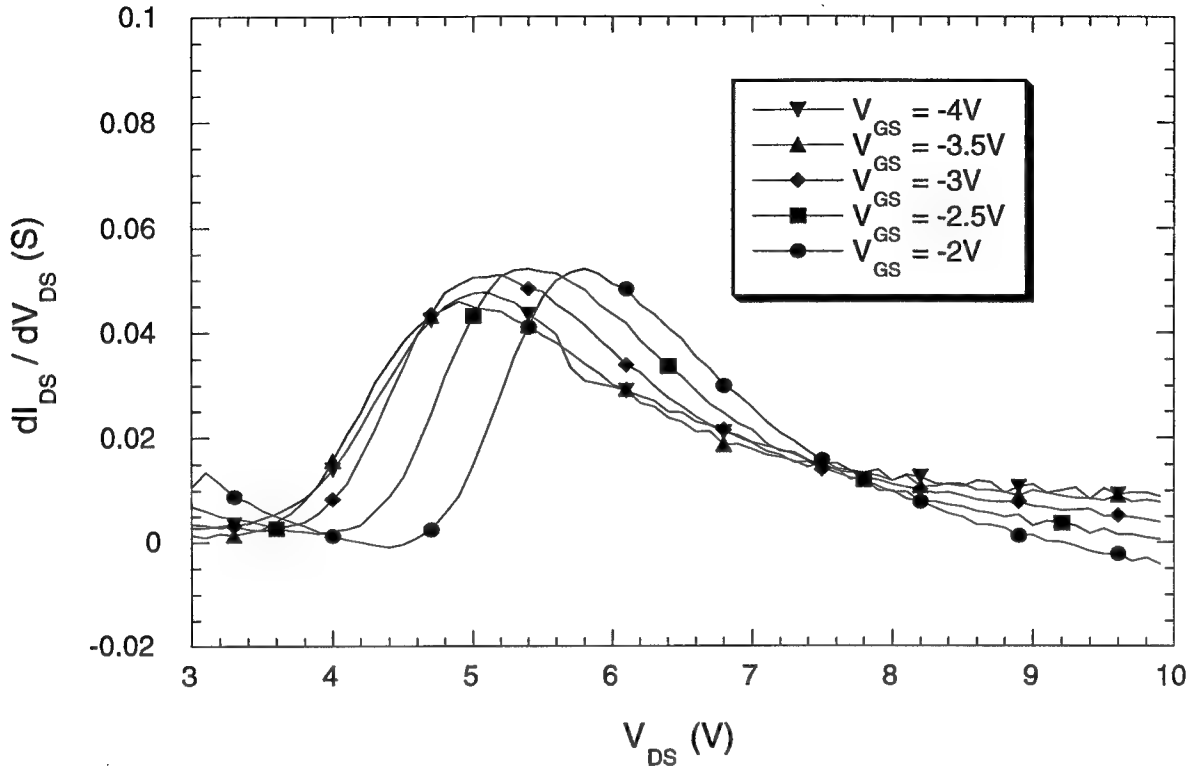


Figure 10a

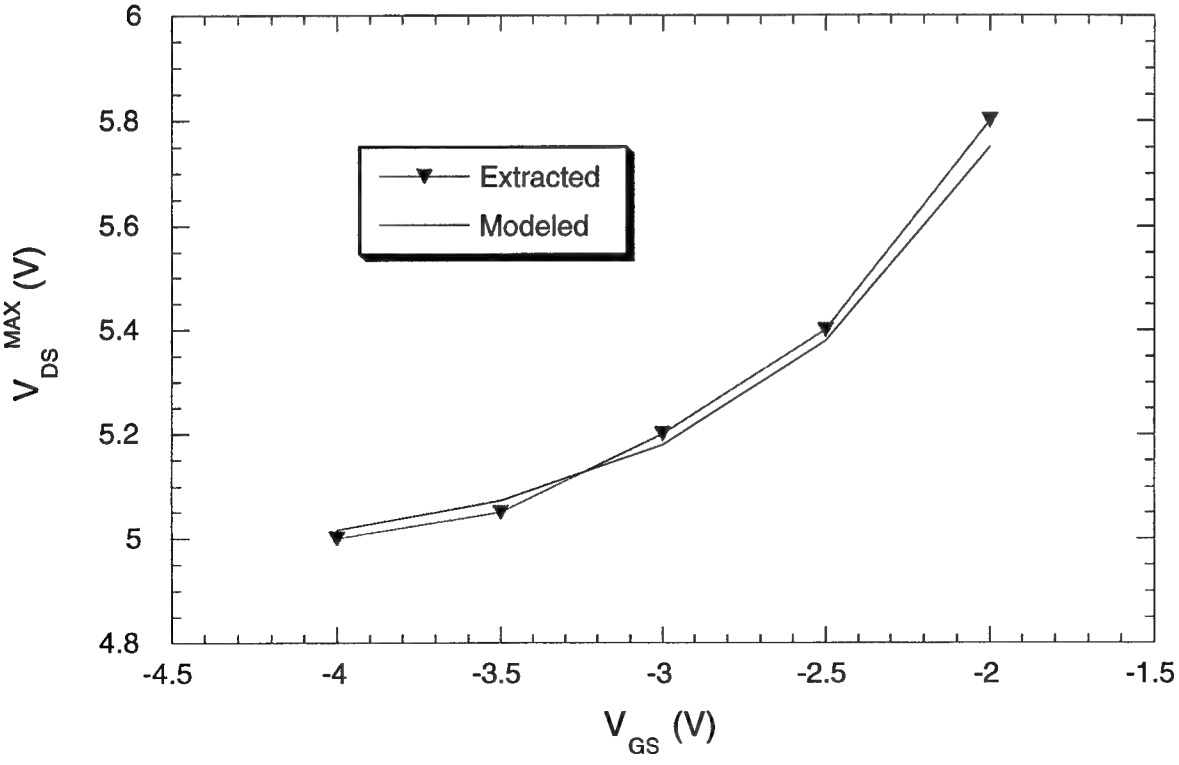
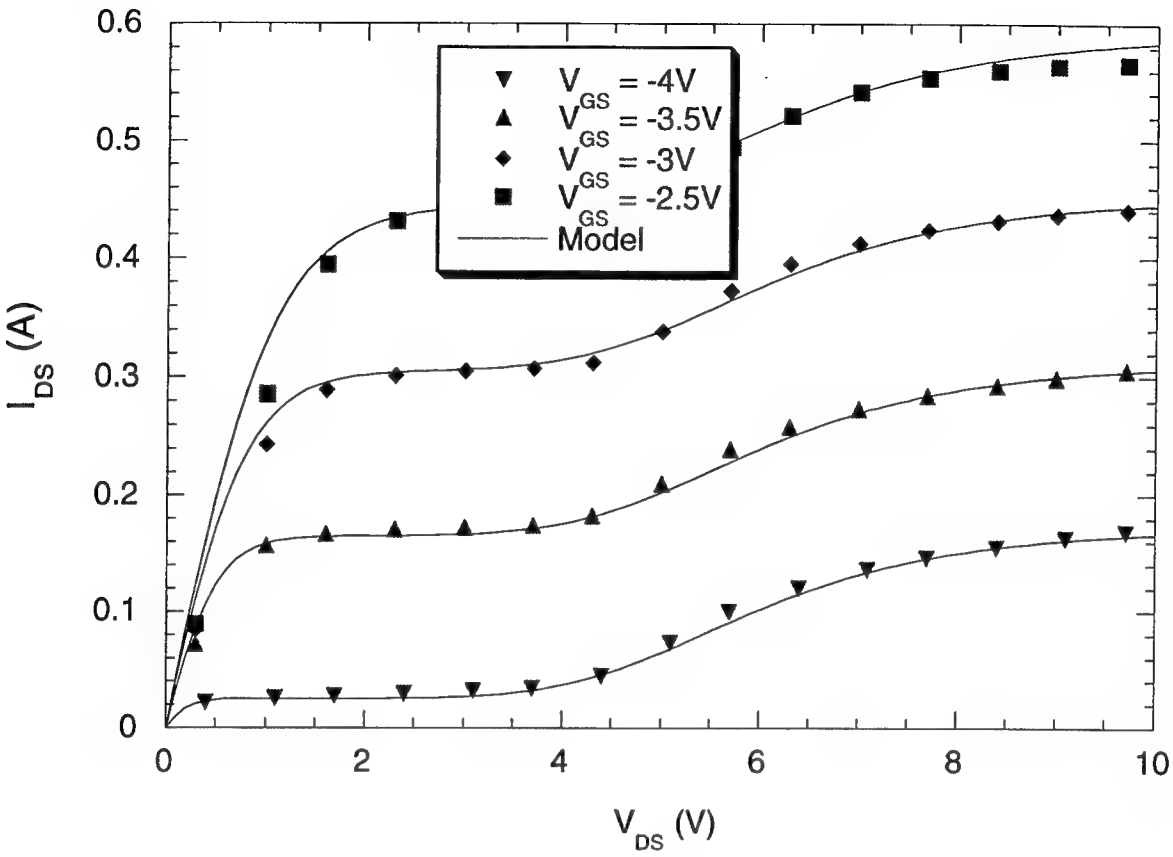


Figure 10b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0.5
0.4
0.3
0.2
0.1
0
I_{DS} (A)
0
2
4
6
8
10
V_{DS} (V)
V_{GS} = -4V
V_{GS} = -3.5V
V_{GS} = -3V
V_{GS} = -2.5V
Model

Figure 11

Submitted Abstract for IEEE Topical Workshop on Power Amplifier for Wireless Communications 2001

POWER AND NOISE CHARACTERIZATION OF ALGAN POWER HEMTS IN PRESENCE OF SELF-HEATING EFFECTS

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ABSTRACT

Power amplifiers that operate at microwave frequencies are key elements for phased array antennas and base stations. With its high breakdown voltage and its high-saturated electron velocity, GaN appears to be a good candidate for high power microwave transistors. GaN-based FETs offer power densities in the few W/mm range, cutoff frequencies (f_T) above 25 GHz, and maximum frequency of oscillation (f_{MAX}) beyond 30 GHz.

Typically AlGaN HEMTs are grown on GaN and SiC substrates that offer a thermal conductivity comparable to the one of Si ($1 - 3$ W.cm^{-1}.K^{-1}). The power densities present in GaN power FETs is large and the overall power cannot be completely dissipated throughout the substrate. As a consequence AlGaN HEMTs suffer from self-heating effects. These effects perturb measurement results and reduce the lifetime of the devices under continuous mode of operation.

We present in this abstract a complete on-wafer characterization of AlGaN power HEMTs. DC, power and noise performances are discussed in details to give an in depth understanding of the major role played by the bias in devices that exhibit self-heating effects. Source-pull and load-pull measurements were carried out under pulsed conditions to characterize the devices in high power regime.

Fig.1 shows drain current characteristics of a 2-finger GaN HEMT (L_G = 0.35µm, W_G = 2 x 125µm). At high gate bias, the drain current decreases with increasing drain voltage demonstrating the presence of heating effects in the device. In this experiment we considered three different condition of operation: low noise (V_{DS} = 10V, V_{GS} = 0V), high output power (V_{DS} = 35V, V_{GS} = 0V), and high efficiency (V_{DS} = 35V, V_{GS} = -2.5V). The 3 dots in Fig.1 show the flowing drain current for those bias conditions under pulse mode of operation (signal period = 300µs and duty-cycle = 1%). We observe that there is a significant difference between continuous and pulse measurement results when operating under high bias condition. Pulsing the bias reduces the junction temperature and therefore reduces the importance of self-heating effects.

Evolution of DC-current characteristics over a time frame of 10 minutes under a bias condition that drives the device into a heat regime (V_{DS} = 35V, V_{GS} = 0V) is shown in Fig. 2. The drain current drops by about 1%, while the gate current increases by almost 30%, most of it during the first 100 seconds. Such an increase in gate current under continuous condition tells that over time the breakdown voltage degrades. Similar measurement with a bias that put the device into a quasi-isothermal environment (V_{DS} = 35V, V_{GS} = -2.5V) gives a fluctuation of gate current of about 1.5%.

Fig. 3 illustrates the pulse-load-pull system used for power measurements. It allows pulsing the gate, the drain, and the RF signal. A 10W TWT amplifier is used to drive the devices into saturation. Source-pull and load-pull contours were achieved on a 12-finger GaN HEMT (L_G = 0.3µm, W_G = 12 x 125µm) under pulsed condition with a constant input power of 28 dBm to find the optimum matching condition in term of output power. Fig. 4 shows the output power contours versus load gammas at 10GHz and (V_{DS} = 35V, V_{GS} = 0V). And Fig. 5 presents the pulsed RF power characteristics of the device set to its optimum source and load impedances. A 3.4W/mm power density was achieved at the 1dB compression point.

Finally, the 4 noise parameters of a 2-finger device were extracted at the three different conditions of operation from 2 to 15GHz. At 8GHz the minimum noise figure (F_{MIN}) for the low noise, high efficiency and high power regime of operation was respectively 2.61 dB, 3.82 dB and 8.32 dB, the noise resistance (R_N) was 189.5 Ω, 55.4 Ω, and 140 Ω, and the associated optimum source impedance shifts toward the inside of the smith chart. Fig. 6 illustrates the noise figure versus source admittances at 8GHz for V_{DS} = 10V and V_{GS} = 0V.

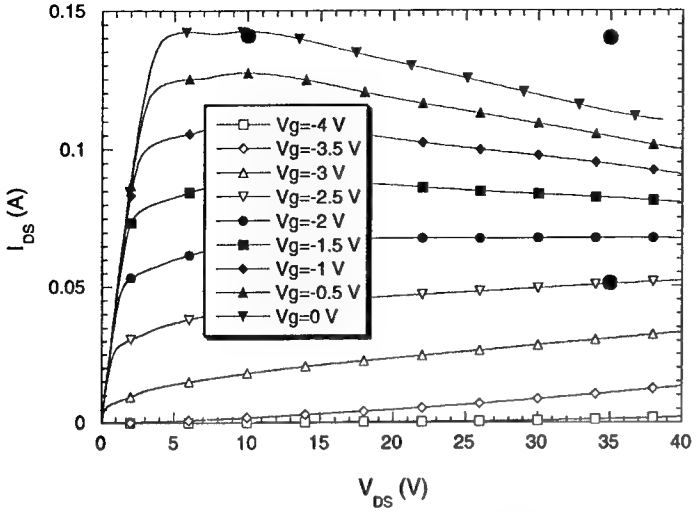

Fig. 1: DC-IV characteristics of a 2-finger device.

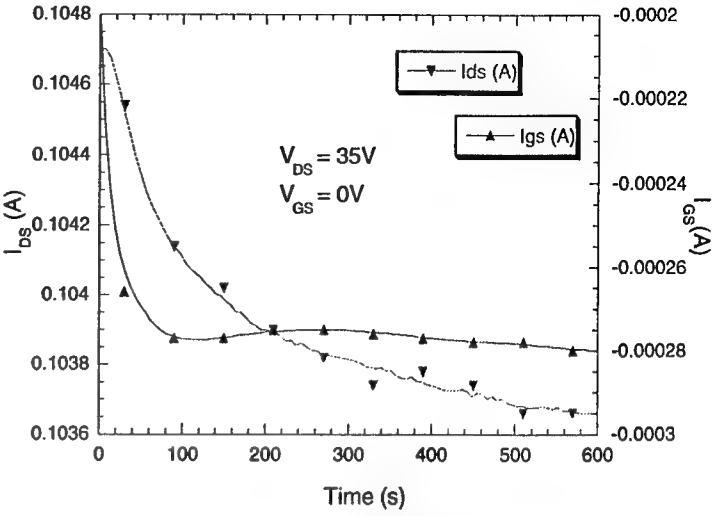

Fig. 2: Evolution over time of DC current characteristics.

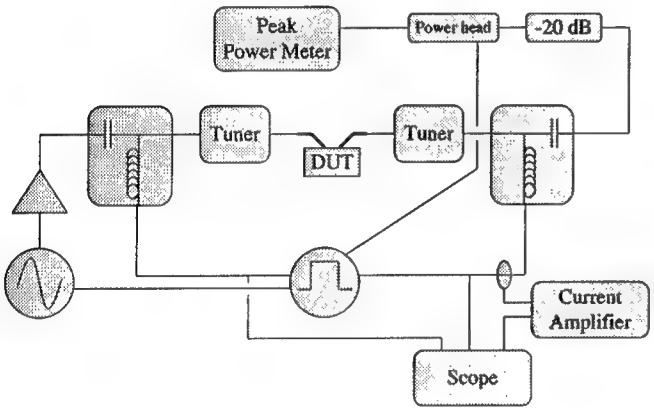

Fig. 3: Schematic of the pulsed source/load – pull system.

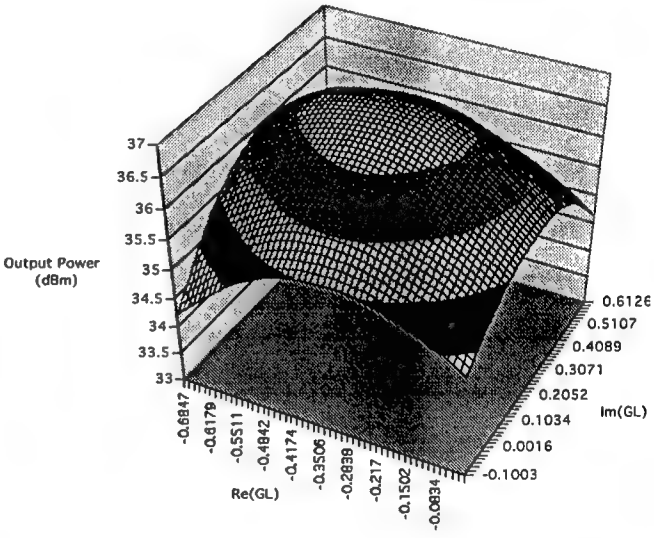

Fig. 4: Output power versus load gammas of a 12-finger device measured under pulsed condition at 10GHz, V_{DS} = 35V, V_{GS} = 0V, P_{IN} = 28 dBm.

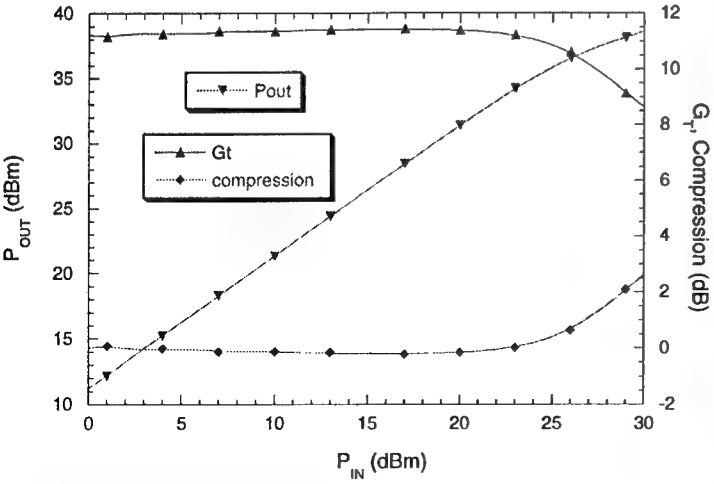

Fig. 5: Pulse power characteristics of a 12-finger device set for optimum transducer gain, at 10GHz, V_{DS} = 35V, and V_{GS} = 0V.

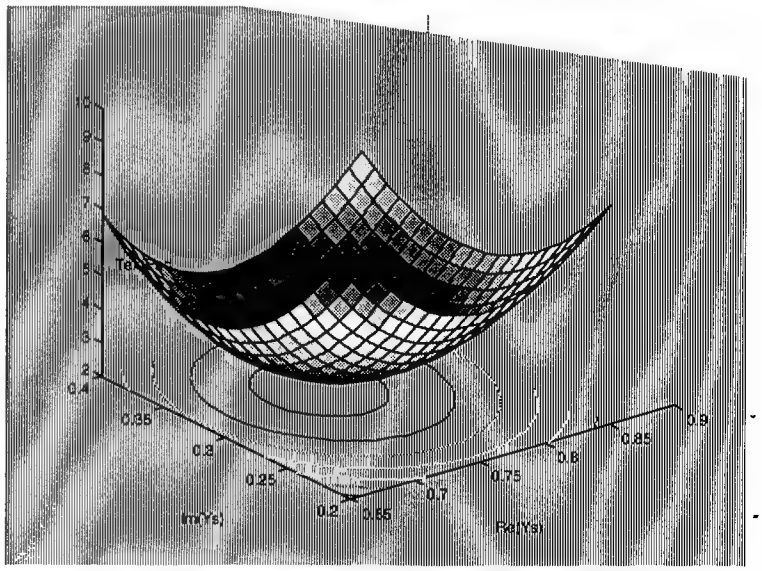

Fig. 6: Noise figure versus source admittances of a 2-finger device, at 8GHz, V_{DS} = 10V, and V_{GS} = 0V.

STUDY OF SELF-HEATING EFFECTS AND TEMPERATURE-DEPENDENT MODELING AND PULSED LOAD-PULL MEASUREMENTS ON GAN HEMTS

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Keywords : Microwave Power FETs, GaN HEMTs, Self-Heating Effects, Modeling, Pulsed Load-Pull.

ABSTRACT

On-wafer RF and IV characterizations are performed for the first time on power GaN HEMTs under pulse and continuous conditions at different temperatures. These measurements give an in depth understanding of self-heating effects and allow one to investigate the possibility of improving heat dissipation mechanisms. A pulsed load-pull system that measures the power gain of the DUT under pulsed RF and bias condition has been developed. To the best of our knowledge, this is the first time that the reflected power at the DUT is measured under pulse mode of operation. Additionally, an improved small-signal model for power GaN HEMT that incorporates the geometry of the device is developed at various temperatures. This is the basis for empirical large-signal modeling.

I- INTRODUCTION

The wireless communication market is growing rapidly and there is a great demand for high power transistors for applications such as phased array antennas and base stations. Today, available power transistors are in the 1W/mm range. Candidates to fill the need for higher output power are Si-LDMOS, and SiC/GaN-based transistors. They offer power densities in the few W/mm range because of their high breakdown voltage [1-7]. GaN-based compared to SiC-based transistors and Si-LDMOS, offers higher cut-off frequencies and maximum frequencies of oscillation ($f_T \approx 25$ GHz, and $f_{MAX} \approx 33$ GHz) [2,4,5].

Pulsed RF and bias measurement systems have been developed to overcome self-heating effects that perturb measurements performed with traditional continuous characterization systems. Such systems allow one to understand the ideal characteristics of a device, and build accurate models for applications that work under pulsed mode of operation such as TDMA. The

study of power devices under pulsed conditions and under different temperatures of operation allows one to understand the thermal behavior and to answer the question of whether or not improvements in heat sinks will ameliorate the device's characteristics. Additionally, studying devices under these conditions enables one to build more robust models that help understand the device physics [6,8,9,10].

The design of RF circuits requires reliable and accurate nonlinear models. During the past 15 years most of the work in the RF nonlinear modeling area has essentially been focused on GaAs MESFETs /HEMTs and Si MOSFETs [11,12]. Improvements in the models have progressively been made to predict more accurately the fundamental frequency, as well as harmonics and intermodulation distortion at different bias conditions, temperatures and terminations. As a result, nonlinear empirical models incorporate a large number of fitting parameters and external circuit elements [11]. RF nonlinear modeling methods of GaN HEMTs can be derived from techniques applied to GaAs and Si FETs.

In this work we present on-wafer measurement results featuring IV, S-parameters, and load-pull characteristics at different temperatures. Both IV and RF power characteristics are achieved in continuous and pulsed modes. Additionally a small-signal model that operates up to 15GHz has been extracted for different bias conditions and at various temperatures of operation, enabling large-signal transistor modeling.

This paper is organized as follows. Section II presents details of the measurement techniques; Section III shows the study of self-heating effects through DC/Pulsed IV and small-signal RF characterization with the temperature of operation as an additional parameter. Modeling of GaN HEMTs for different temperatures is presented in Section IV, and the results of cryogenic load-pull measurements are presented in Section V, followed by a conclusion.

II- Experimental Setup

On-wafer measurements have been carried out at temperatures as low as 65K using a custom made cryogenic probe station. The cryogenic probing system (Fig.1) contains ports for RF and DC cables, temperature sensors, vacuum pumps, coplanar wave-guide probes with manipulators, and a closed-cycle helium refrigerator cold head. The device under test (DUT) is mounted on the cold wafer stage and the test chamber is evacuated to prevent frost build up and large thermal gradients when cooling the chamber.

The experimental setup consists of two pulse bias generators, a frequency source synchronized with the pulse generators, a solid-state power amplifier, and mechanical tuners to control the load and source impedances at the DUT. The current is monitored with a digitizing scope through a current probe. The RF power is monitored with a peak power meter. Measurements are achieved at a gate baseline that is in the pinch-off region of the DUT. Both the drain and RF pulse width are shorter and delayed by a few 100ns in order to be centered in the gate pulse. Fig.2 presents a diagram of the setup used.

An S-parameter calibration of all elements (fixtures, bias tees, couplers, cables, adapters...) is used to retrieve the actual power at the input and output of the DUT. To our knowledge we are the first to measure the reflected power under pulsed conditions and under large-signal mode of operation for various load and source impedances (load-pull measurement setup), allowing us to extract the power gain (G_P) of the DUT in addition to the transducer gain (G_T).

The studied GaN HEMTs are provided by CREE Inc. and are grown on a SiC substrate, with a gate width of 125 μm per finger. Measurements were performed on different devices with various gate lengths (L_G), number of fingers, gate to source lengths (L_{GS}) and gate to drain lengths (L_{GD}).

III- Study Of Self-Heating Effects Through DC/Pulsed IV And Small-Signal RF Characterization At Various Temperatures

Under large drain bias, the device lattice temperature increases and so does the carrier phonon scattering rate, which leads to a drop in the carrier mobility. This effect has been reported to be of great influence in reducing the output conductance of FETs [13], and is commonly referred as "self-heating". Evidence of such effect is a negative slope in $I_{DS}(V_{DS})$. Biasing devices during a short period of time reduces carrier / lattice exchanges and therefore one can control the heat dissipation in the device. Experiments performed using pulsed IV systems support this assumption by showing characteristics free of self-heating [14,15,16].

The lattice temperature is also well known to be of significant influence on the carrier mobility, and therefore on the device characteristics.

We present in this section a study of heating effects in GaN HEMTs through DC/Pulsed IV and small-signal RF characterization at various temperatures of operation.

A- DC/PULSED IV CHARACTERIZATION

The GaN HEMT DC characteristics show an increase in the drain current and the device transconductance while operating at reduced temperature (Fig.3). The improvements are results of an increase in electron mobility [17].

Fig.4 exhibits pulsed-IV measurement characteristics at 300 K for various duty-cycle at 0 V gate bias and a pulse period of 100 μs. By gradually reducing the pulse width the negative slope of the $I_{DS}(V_{DS})$ characteristics diminishes.

Fig.5 compares the drain-to-source current at 300K and 65K under pulsed and continuous mode of operation. Pulsed characteristics are obtained with a signal period of 100 μs, and a pulse width of 1 μs on the drain side. Unlike at 300 K, pulsed and continuous I-V characteristics at T = 65 K correlate for drain voltages larger than 15 V. The mismatch observed at 65 K at low drain voltages has been reported in [18].

Fig.6 shows the temperature effects on DC-$I_{DS}(V_{DS})$ and DC-$I_{GS}(V_{DS})$ characteristics. At any temperature, it is possible to define the drain voltage threshold as the drain voltage value at which the drain current starts to decrease. It is noteworthy that as the temperature decreases, the drain voltage threshold increases. This is interpreted as an extension of the drain voltage range for which the DUT does not suffer from self-heating. At the same time a decrease in the temperature reduces the gate current.

At any bias and temperature condition, it is possible to define the pulse width threshold as the pulse width that leads to a drain current saturation. Fig.7 displays the pulse width threshold for V_{DS} = 45 V, V_{GS} = 0 V, a period of 100 μs, and at several temperatures. We observe that at 150 K, the drain current is saturated at all available pulse widths. This is perceived as an absence of any heating effects. Above 225 K the drain current could not be saturated at any available duty-cycle (the minimum duty-cycle used was 1 %). Therefore, it is possible to say that the pulse width threshold is below 1 μs for temperatures greater than 225 K. For temperatures between 150 K and 225 K saturation of the drain current was observed, and thus a threshold value was extracted. We observed that the threshold value to achieve drain current saturation increases while temperature decreases, meaning that a reduction in the external temperature decreases self-heating effects in the device. Fig.7 also shows the pulse width threshold as a function of temperature for two different bias conditions.

B- SMALL-SIGNAL RF CHARACTERIZATION

S-parameters allow one to study the small-signal device performances. They enable the derivation of the stability factor, the cut-off frequency (f_T), the maximum frequency of oscillation (f_{MAX}), and the load and source stability circles. These extracted parameters help one understand the behavior of devices under large-signal mode of operation. The load and source contours give initial matching conditions for maximum output power and gain.

f_T and f_{MAX} are extracted respectively from the short-circuit current gain (h_{21}) and the maximum available unilateral gain ($G_{A,Max}$) calculated using the following expressions:

$$h_{21} = \frac{-2 \cdot S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}}$$

$$G_{A,Max} = \frac{|S_{21}|^2}{\left(1 - |S_{11}|^2\right) \cdot \left(1 - |S_{22}|^2\right)}$$

Fig.8 shows short-circuit current gain and maximum available gain under different temperature conditions. The cutoff frequency (f_T) and the maximum frequency of oscillation (f_{MAX}) improve while reducing the temperature of operation.

IV- MODELING OF GAN HEMT

A standard Hybrid-Pi topology is used to simulate the characteristics of a GaN HEMT (Gate Width = 125×2μm, L_{GS} = 0.1μm, and L_{GD} = 3μm) from 1GHz to 15GHz over a complete range of bias conditions and temperatures. As shown in the equivalent circuit (Fig.9) the value of 15 parameters are determined to simulate the device characteristics under small-signal operations. The elements outside the dotted box represent the extrinsic part of the device. They come from the metal traces and the probing pads [19]. "ColdFET" measurements in conjunction with an improved equivalent circuit based on geometrical considerations of the device lead to the parasitic element values determination. Intrinsic element values are determined analytically from the intrinsic Y-parameters. Finally a CAD tool is used to optimize all parameters values.

A- EXTRACTION OF PARASITIC ELEMENTS

S-parameters measurements at zero drain bias can be used to determine the device extrinsic parameters because the equivalent circuit is much simpler [19,20].

Parasitic capacitances are obtained from the Y parameters recorded under pinched-off conditions. The small-signal model presented in this paper simulates a highly non-symmetric

device (L_{GS} = 0.1 µm, L_{GD} = 3 µm), and equations from Dambrine *et al.* [19] and White *et al.* [20] yield to negative values for the extrinsic capacitances. The equivalent circuit proposed in [19] and [20] under pinched-off conditions considered a uniform repartition of the fringing capacitance C_B under the gate. Two scaling coefficients, based on the geometry of the device, are added to take into account the asymmetry of the device. Fig.10a shows a schematic cross section of the transistor at zero drain bias showing the physical origin of the scaling coefficients, and Fig.10b presents a complete equivalent circuit under such bias conditions. A gate centered with the drain and the source would lead to two equal scaling coefficients, and therefore to the model proposed by Dambrine *et al.*. By neglecting the influence of the inductances and the resistances, the imaginary part of the Y-parameters of the previous circuit are given by:

$$\mathrm{Im}(Y_{11}) = j.\omega.(C_{PG} + (a+b).C_B)$$
$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j.\omega.a.C_B$$
$$\mathrm{Im}(Y_{22}) = j.\omega.(C_{PD} + a.C_B)$$

where a and b are the two scaling coefficients. Fig.11 presents the absolute values of the Y-parameters imaginary part measured at zero drain bias and under pinched-off condition. The extracted capacitances values are C_{PD} = 34.6 fF, and C_{PG} = 44.22 fF (a = 3 and b = 0.1).

Parasitic inductances and resistances are obtained from measurements at zero drain bias and under forward gate bias conditions [19]. Under such bias conditions the Z-parameters can be expressed as :

$$Z_{11} = R_S + R_G + \frac{R_C}{3} + \frac{n.k.T}{q.I_G} + j.\omega.(L_S + L_G)$$
$$Z_{12} = Z_{21} = R_S + \frac{R_C}{2} + j.\omega.L_S$$
$$Z_{22} = R_S + R_D + R_C + j.\omega.(L_S + L_D)$$

where R_C represents the channel resistance.

The extrinsic inductances can therefore be extracted from the imaginary part of the Z-parameters. Fig.12 shows results derived from S-parameters measurements. The calculated parasitic inductance values are L_S = 22 pH, L_D = 23.1 pH and L_G = 23.4 pH.

The real part of Z_{12} and the real part of Z_{22} (Fig.13) lead to 2 equations involving the parasitic resistances as well as the channel resistance. A third relation is obtained by knowing the real part of Z_{11} under various gate conditions (Fig.14a and Fig.14b). An additional relation

required for unequivocal resistance determination can be obtained from various methods [19]. In this model, the parasitic resistances are expressed as a function of the channel resistance (Fig.15), and a range of possible values for R_C is determined by considering that all resistances value must be kept positive. An initial value for the extrinsic resistances is then determined by taking the channel resistance value in the middle of its range.

B- EXTRACTION OF INTRINSIC ELEMENTS

The intrinsic elements can be analytically determined from the intrinsic Y-parameters [21] obtained after deembedding the parasitic elements from the measured S-parameters through a series of matrix operations [19]. Fig.16a presents the extracted transconductance G_M on a complete bias range at T = 150K and T=300K. It illustrates the improvement of the GaN HEMT characteristics while operating at reduced temperature, confirming results obtained from DC-IV measurements. Fig.16b shows an increase of the gate to source capacitance on a wide bias range when the temperature of operation is reduced from 300K to 150K.

C- RESULTS

A design tool is used to tune the final value of extrinsic and intrinsic parameters. The extrinsic parameters values are finally L_G = 23.4 pH, L_D = 23.1 pH, L_S = 22 pH, R_G = 3.5 Ω, R_D = 15 Ω, R_S = 5 Ω, C_{PG} = 36.9 fF, and C_{PD} = 27.9 fF. Small-signal simulations are performed from 1GHz to 15GHz at V_{GS} = -1 V and V_{DS} = 30 V at T = 150K (Fig.17a), and at T = 300K (Fig.17b). Table 1 summarizes the intrinsic element values at both temperatures.

V- LOAD-PULL CHARACTERIZATION OF GAN HEMTS

As presented earlier, self-heating occurs under large drain bias and at high drain current, in continuous mode of operation. The pulsed load-pull system allows us to measure RF power characteristics of a device under various load and source terminations and under pulsed RF and bias conditions enabling us to know the power characteristics of power devices in a heat free mode of operation. We propose in this section to study the influence of self-heating on RF power characteristics.

Fig. 18 shows the RF power performance into 50ohm termination of a GaN HEMT sample when operated at reduced lattice temperature. Measurements are achieved under pulsed and CW mode of operation at V_{GS} = 0 V and V_{DS} = 30 V. As the temperature decreases the heating effects become less important resulting in little difference between CW and pulsed RF/bias power

measurements. The pulsed power measurements are achieved with a 5μs pulse width on the gate side, a 3μs pulse width for the drain, and a 2μs pulse width for the RF signal (f = 10GHz). While the absence of negative slope in $I_{DS}(V_{DS})$ at V_G = -2V shown in the inset of Fig.18 is characteristic of a heat-free environment, the negative output conductance for V_{DS} greater than 12 V at V_G = 0 V tells us that self-heating is not negligible.

Fig.19 illustrates the transducer and power gain of the device under both pulsed and continuous mode of operation tuned for maximum output power at the 1dB compression point. Optimum load and source impedances were determined under pulsed condition. The pulsed power measurements are achieved with a 3.4μs pulse width on the gate side, a 3.2μs pulse width for the drain, and a 3μs pulse width for the RF signal (f = 10GHz). The duty-cycle was set to 1%. It is the first time that the reflected power is measured under pulsed condition. The device exhibits an improvement of gain when operating under pulsed conditions. Additionally Fig. 19 shows the drain-to-source current under pulsed and continuous regime. As expected, the drain current is larger under pulsed mode, because the device operates in a heat free regime.

VI- CONCLUSION

In addition to detailed on-wafer measurements results of DC-IV, Pulsed-IV, and S-parameters, a novel pulsed load-pull system featuring reflected power measurements has been built and utilized to measure for the first time RF power characteristics of GaN HEMTs at various temperatures of operation under pulsed condition. These measurements allow the understanding of self-heating effects in GaN-based transistors and the possibility for device structure improvement resulting in better device performance. The measurement results give an in depth understanding of the device behavior and are the basis for robust device modeling. A small-signal model that takes into account the device geometry for parasitic extraction has also been developed at different temperatures of operation.

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FIGURE CAPTIONS

FIG. 1 : Photograph of the cryogenic microwave probe station.

FIG. 2 : Schematic of the measurement system.

FIG. 3 : Transconductance and drain current versus V_{GS} for various temperatures at V_{DS} = 30 V.

FIG. 4 : Drain current for various duty cycles at V_{GS} = 0 V, at 300 K.

FIG. 5 : Drain current at V_{GS} = 0 V under pulsed and continuous conditions at T = 65 K and T = 300 K.

FIG. 6 : Drain and gate current for various temperatures at V_{GS} = 0 V.

FIG. 7 : Drain current versus pulse width for pulse width threshold determination (isothermal environment) at various temperatures.

FIG. 8 : Short circuit current gain and maximum available gain at different temperatures (300, 250, 150 K).

FIG. 9 : Equivalent circuit diagram of an HEMT used for parameter extraction and modeling.

FIG. 10A : Schematic cross section of HEMT at V_{DS} = 0V showing physical origin of scaling elements for equivalent circuit under pinch-of condition.

FIG. 10B : Equivalent circuit of pinched-off FET at V_{DS} = 0V.

FIG. 11 : Imaginary part of Y-parameters versus frequency for HEMT device biased beyond pinch-off at V_{DS} = 0V, for parasitic capacitances determination.

FIG. 12 : Imaginary part of Z-parameters versus frequency under forward gate bias voltage and zero drain bias voltage for parasitic inductances determination.

FIG. 13 : Real part of Z-parameters versus frequency under forward gate bias voltage and zero drain bias voltage for parasitic resistances determination.

FIG. 14A : Real part of Z_{11} versus frequency under various forward gate bias voltage and zero drain bias voltage for parasitic resistances determination.

FIG. 14B : Real part of Z_{11} at zero drain bias versus $1/I_G$ for parasitic resistances determination.

FIG. 15 : Parasitic resistances versus channel resistance.

FIG. 16A : Extracted transconductance G_M versus gate and drain bias at T = 150K and T = 300K.

FIG. 16B : Extracted gate to source capacitance C_{GS} versus gate and drain bias at T = 150K and T = 300K.

FIG. 17A : Comparison of measured and modeled S-parameters at V_{DS} = 30V, V_{GS} = -1V, f = 1 – 15 GHz, T = 150K.

FIG. 17B : Comparison of measured and modeled S-parameters at V_{DS} = 30V, V_{GS} = -1V, f = 1 – 15 GHz, T = 300K.

FIG. 18 : Output power versus frequency under pulsed and continuous conditions into 50 Ohms termination at T = 150 K and T = 300 K (V_{DS} = 30 V, V_{GS} = 0 V). The insert shows $I_{DS}(V_{DS})$ data at 300 K, at V_{GS} = 0 V and V_{GS} = -2 V, with V_{DS} up to 35 V.

FIG. 19 : Pulsed (dashed lines) and continuous (solid lines) RF power measurement results into terminations for maximum output power, at f = 10GHz, V_{DS} = 30 V, V_{GS} = 0 V, and T = 300K.

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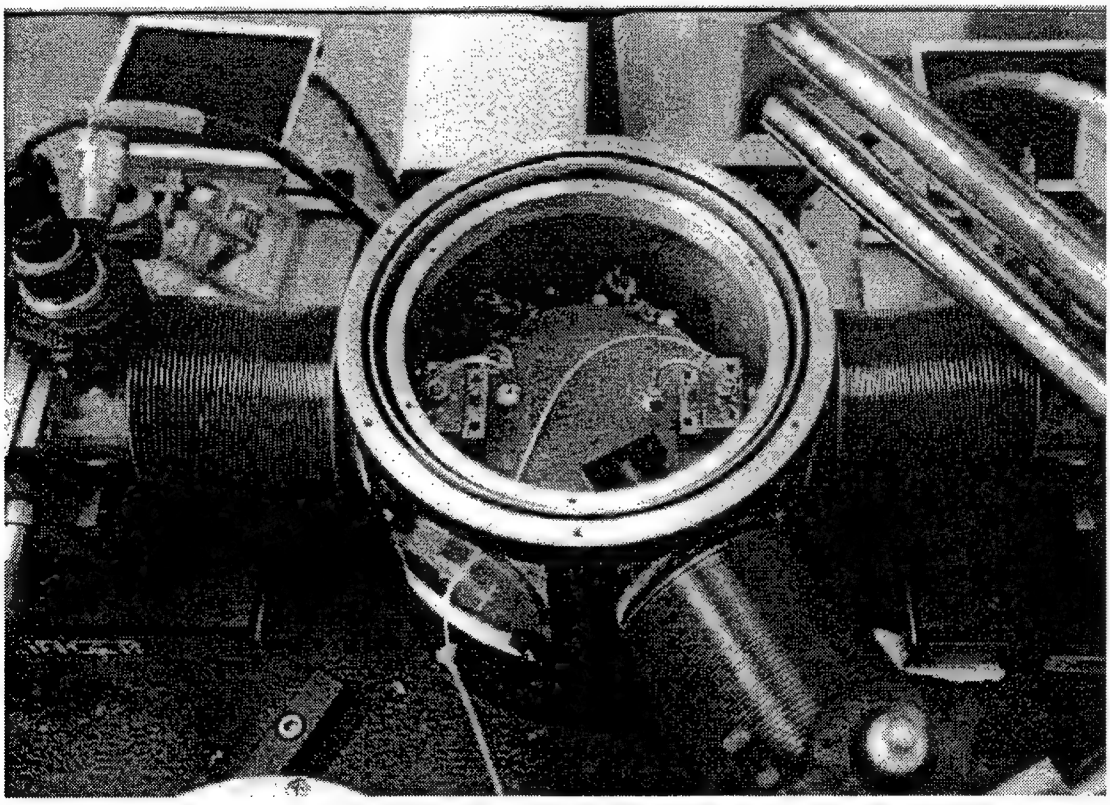

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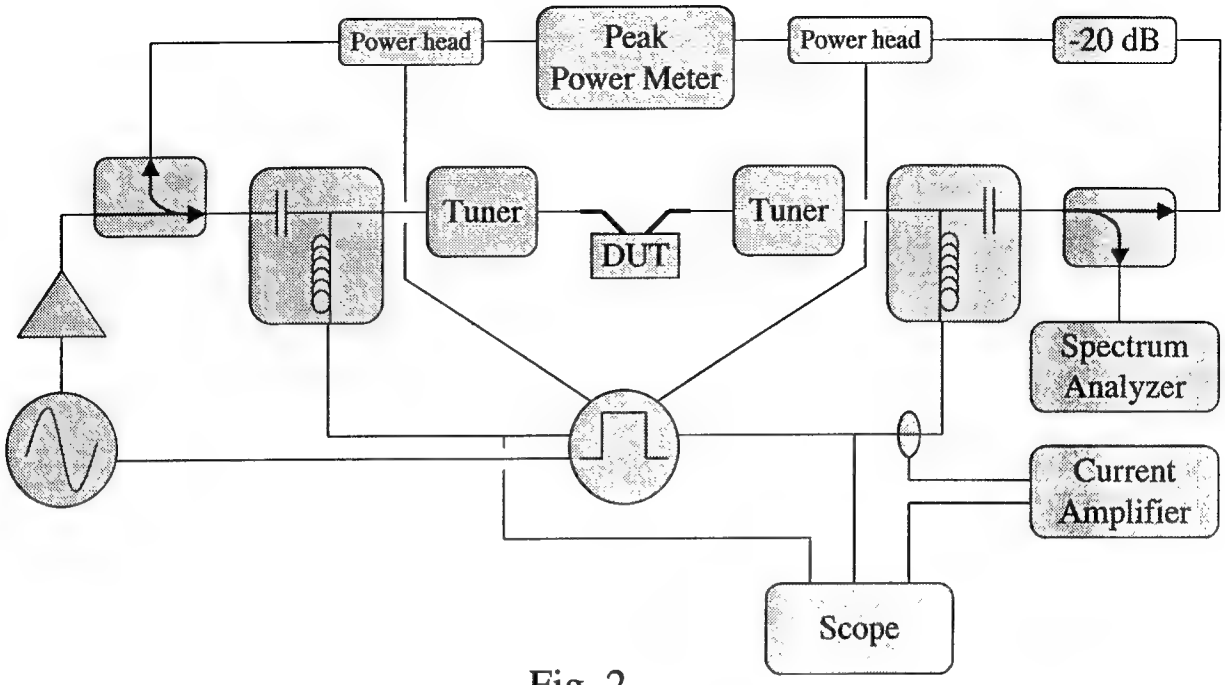
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Fig. 2

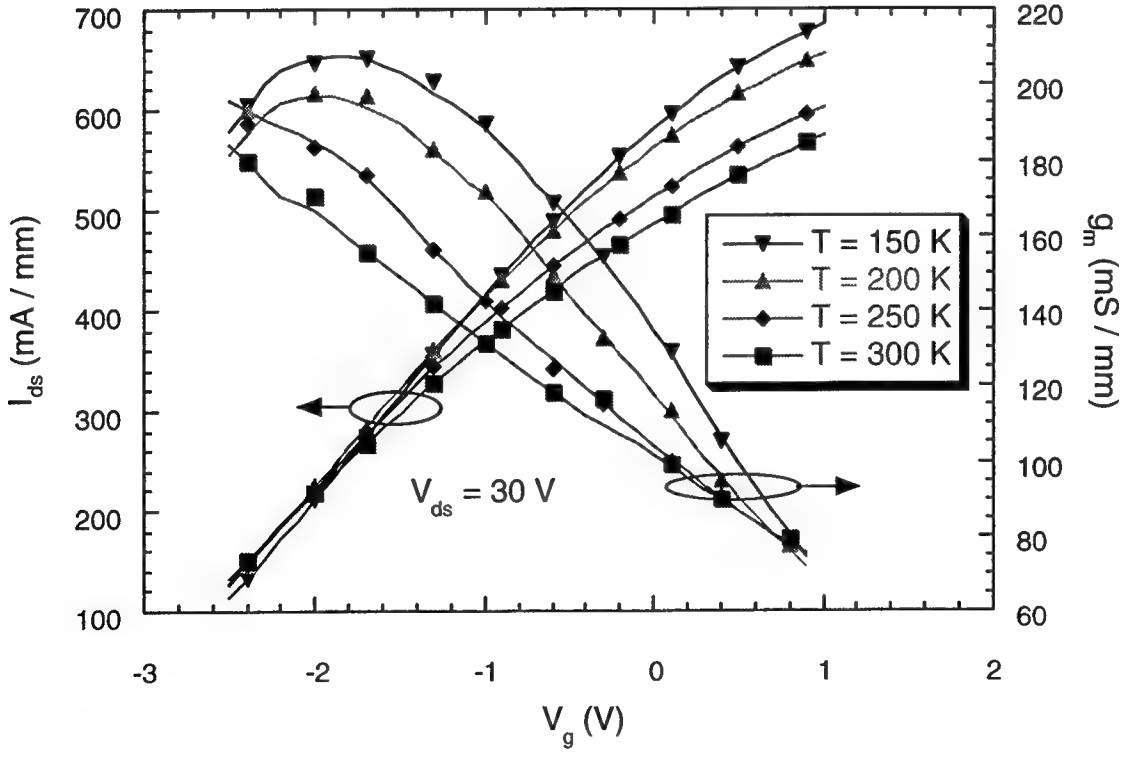
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Fig. 3

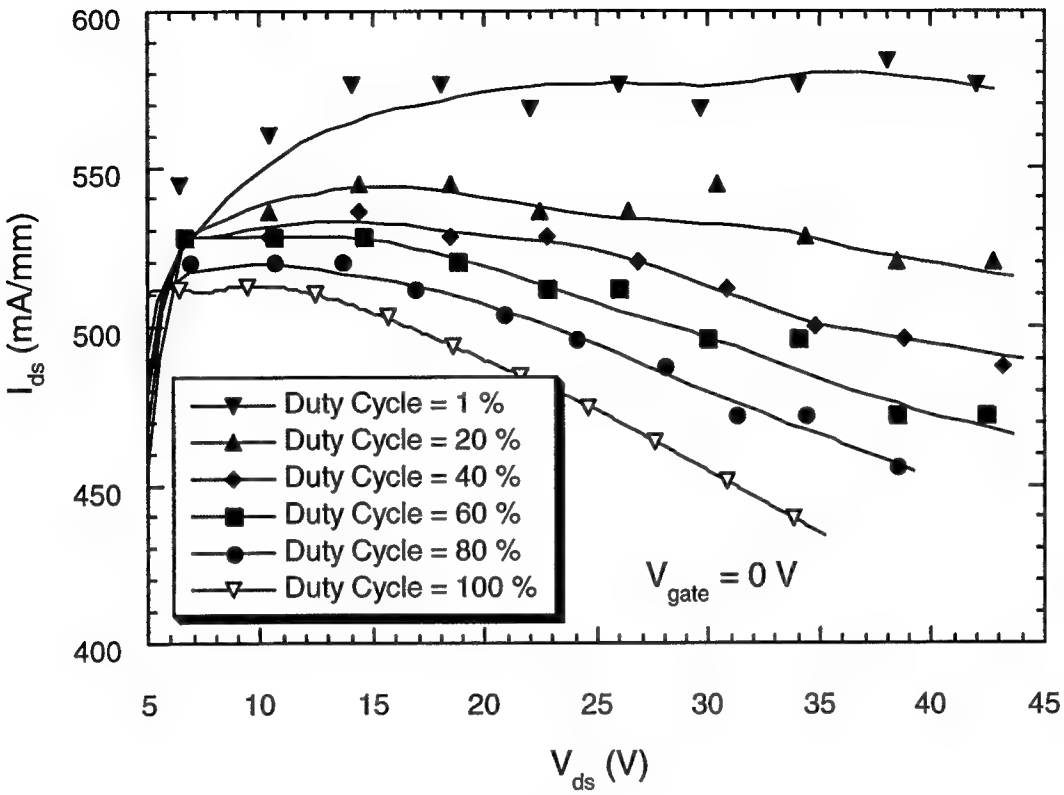
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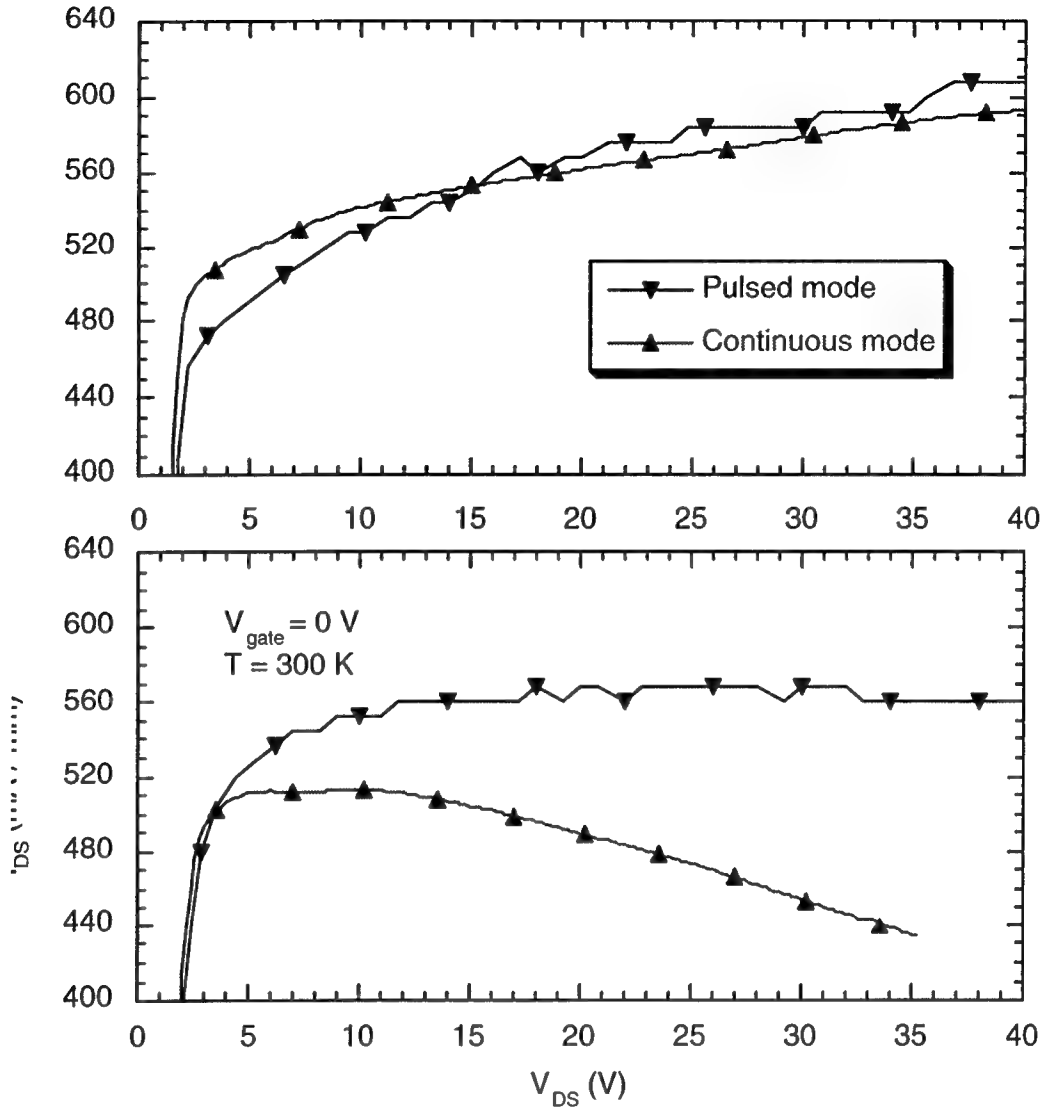
Fig. 4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10
15
20
25
30
35
40
Pulsed mode
Continuous mode
V_{gate} = 0 V
T = 300 K
V_{DS} (V)

Fig. 5

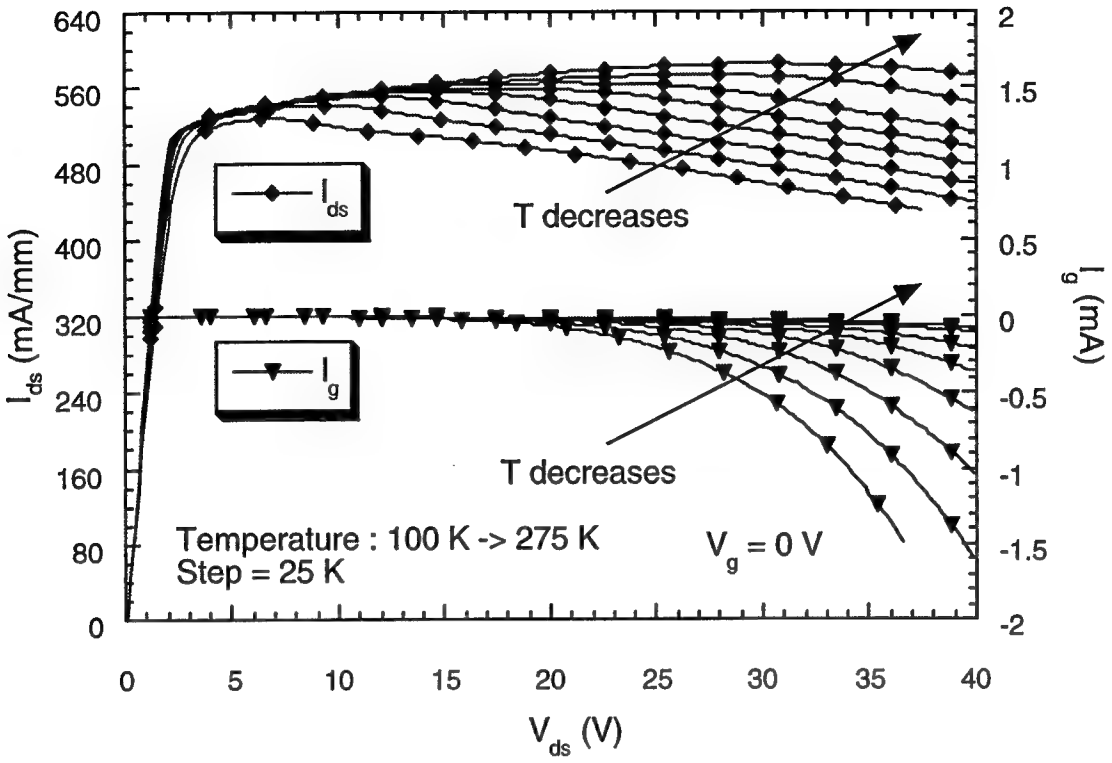
640
560
480
400
320
240
160
80
0
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
I_{ds} (mA/mm)
I_g (mA)
I_{ds}
I_g
T decreases
T decreases
Temperature : 100 K -> 275 K
Step = 25 K
V_g = 0 V
0
5
10
15
20
25
30
35
40
V_{ds} (V)

Fig. 6

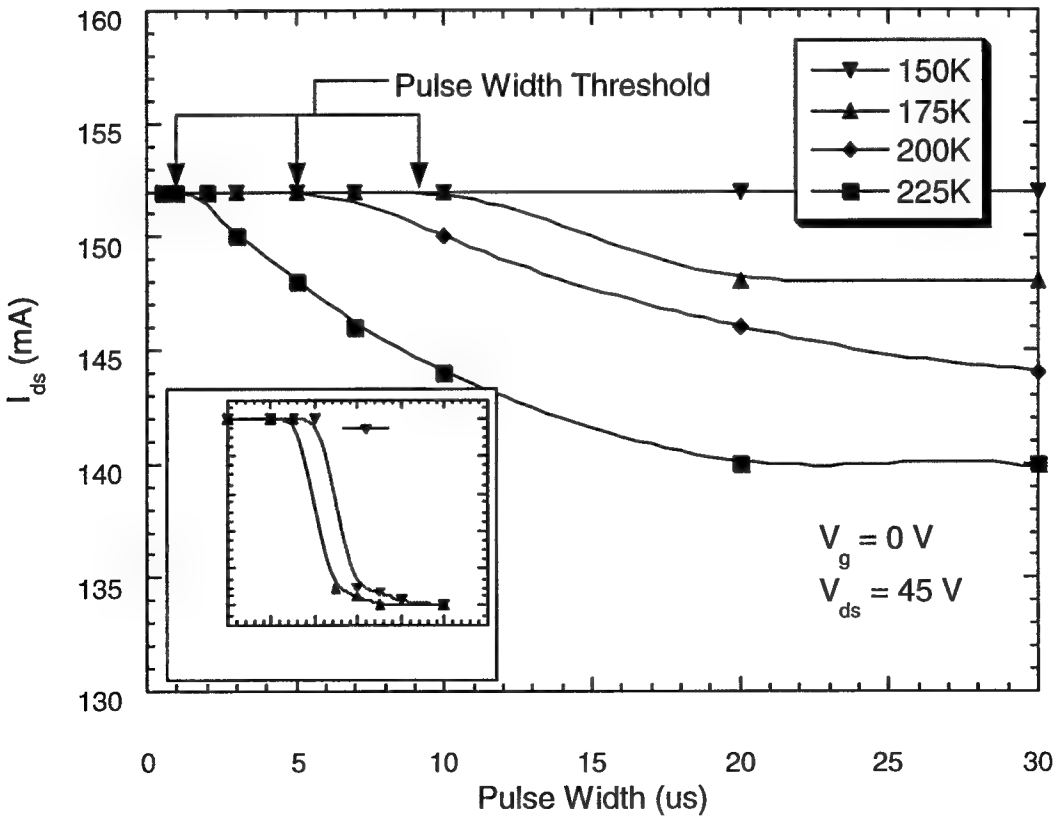
160
155
150
145
140
135
130
I_{ds} (mA)
Pulse Width Threshold
150K
175K
200K
225K
V_g = 0 V
V_{ds} = 45 V
0
5
10
15
20
25
30
Pulse Width (us)

Fig. 7

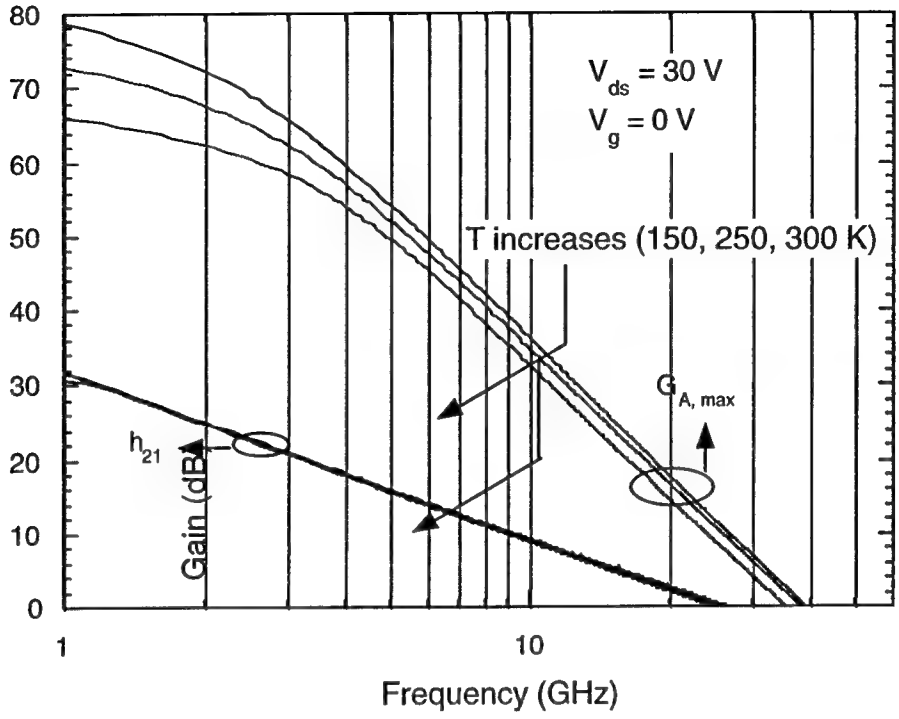
80
70
60
50
40
30
20
10
0
1
10
Frequency (GHz)
Gain (dB)
V_{ds} = 30 V
V_g = 0 V
T increases (150, 250, 300 K)
$G_{A, max}$
h_{21}

Fig. 8

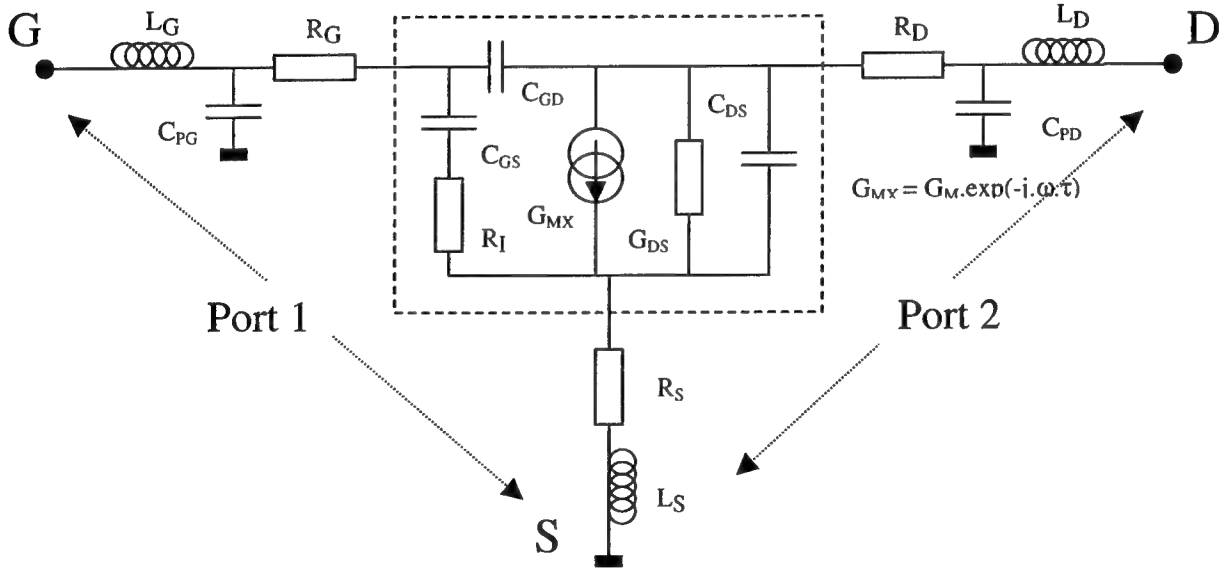
G
L_G
R_G
C_{PG}
C_{GD}
C_{GS}
R_I
G_{MX}
C_{DS}
G_{DS}
R_D
L_D
C_{PD}
D
$G_{MX} = G_M.\exp(-i.\omega.\tau)$
Port 1
Port 2
R_S
L_S
S

Fig. 9

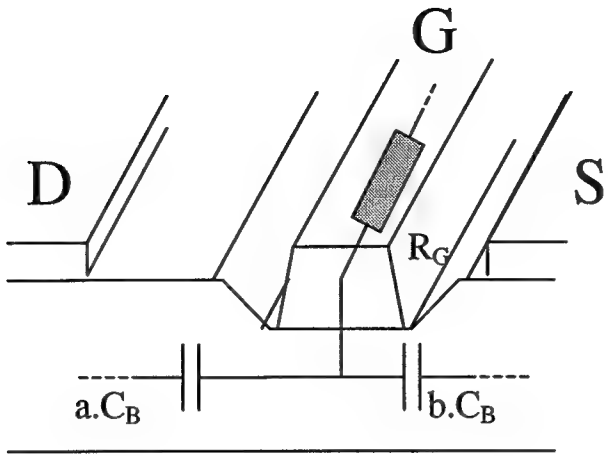

Fig. 10a

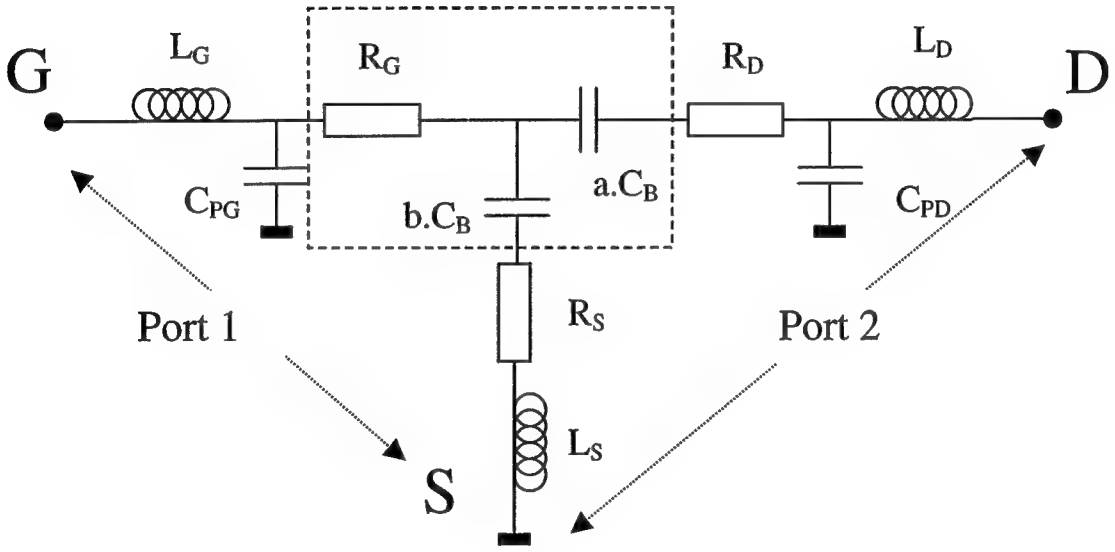

Fig. 10b

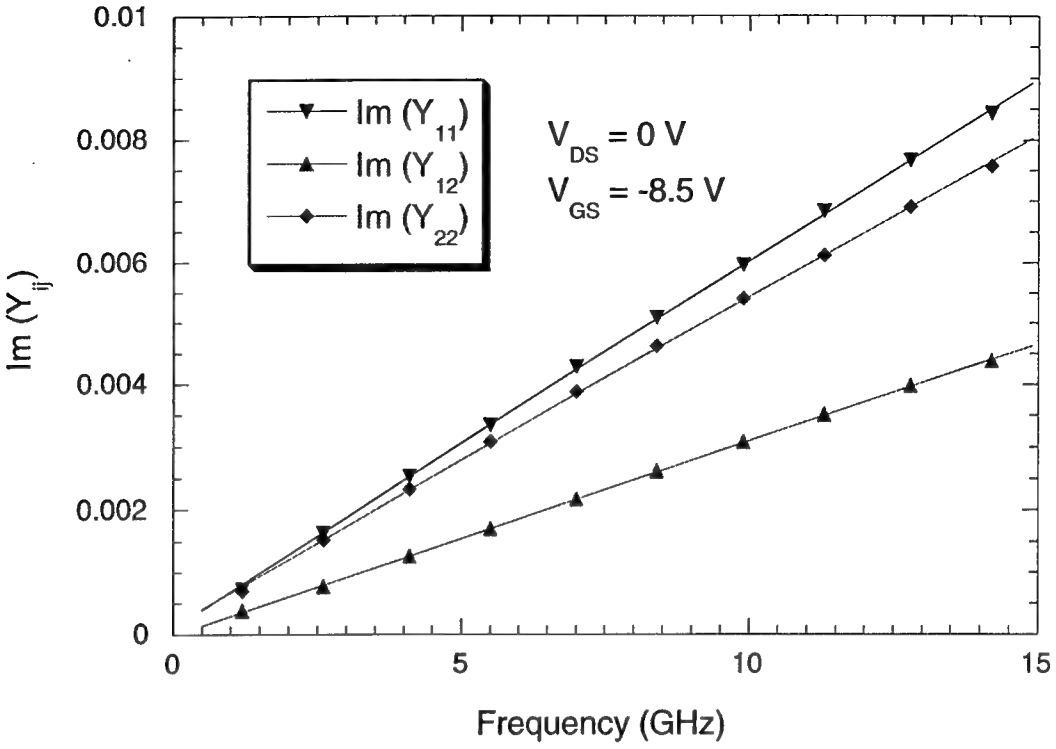
0.01
0.008
0.006
0.004
0.002
0
Im (Y_ij)
Im (Y_11)
Im (Y_12)
Im (Y_22)
V_DS = 0 V
V_GS = -8.5 V
0
5
10
15
Frequency (GHz)

Fig. 11

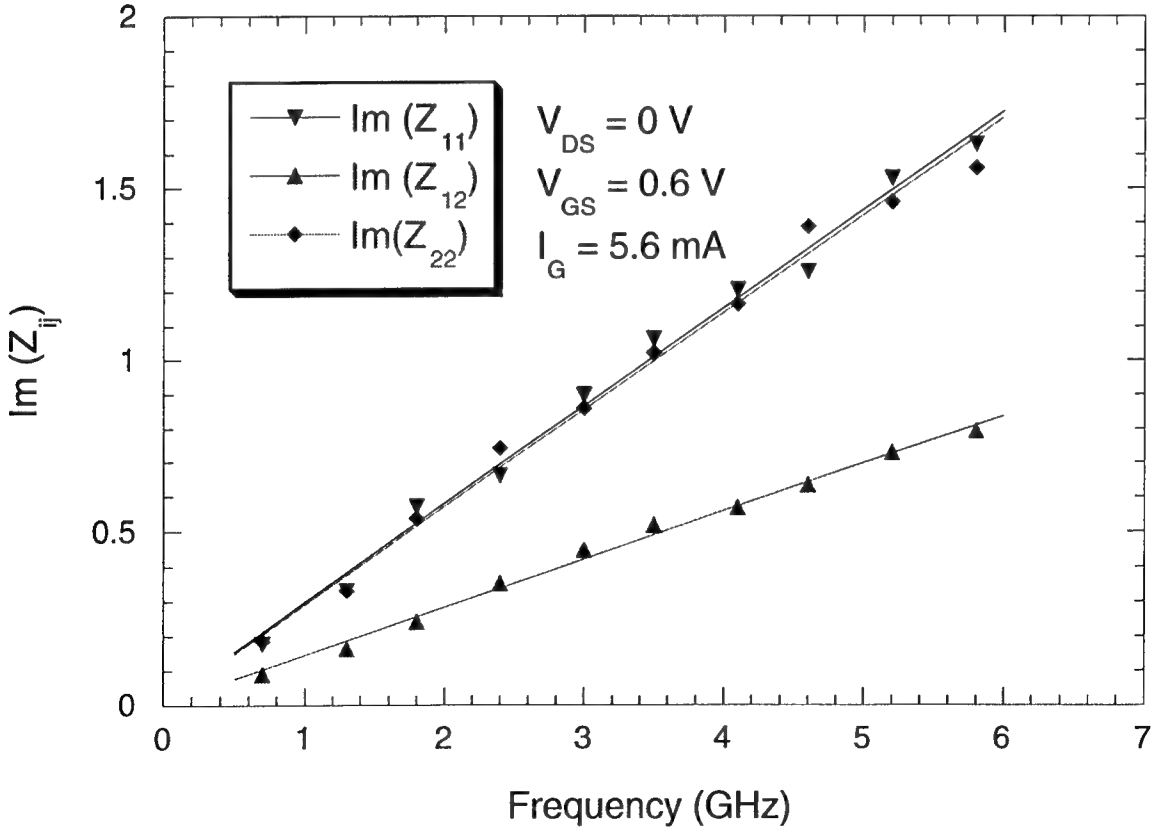
2
1.5
1
0.5
0
Im (Z_ij)
Im (Z_11)
Im (Z_12)
Im(Z_22)
V_DS = 0 V
V_GS = 0.6 V
I_G = 5.6 mA
0
1
2
3
4
5
6
7
Frequency (GHz)

Fig. 12

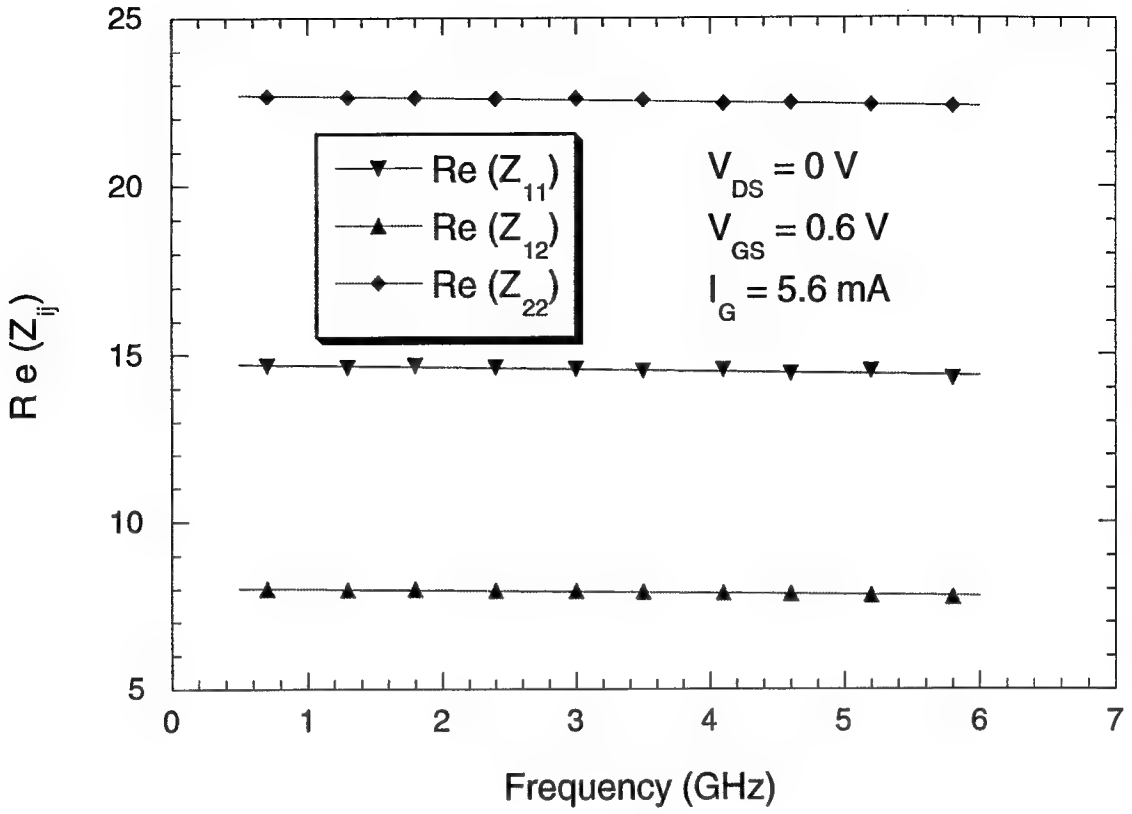
25
20
15
10
5
0
1
2
3
4
5
6
7
Re (Z_ij)
Frequency (GHz)
Re (Z_11)
Re (Z_12)
Re (Z_22)
V_DS = 0 V
V_GS = 0.6 V
I_G = 5.6 mA

Fig. 13

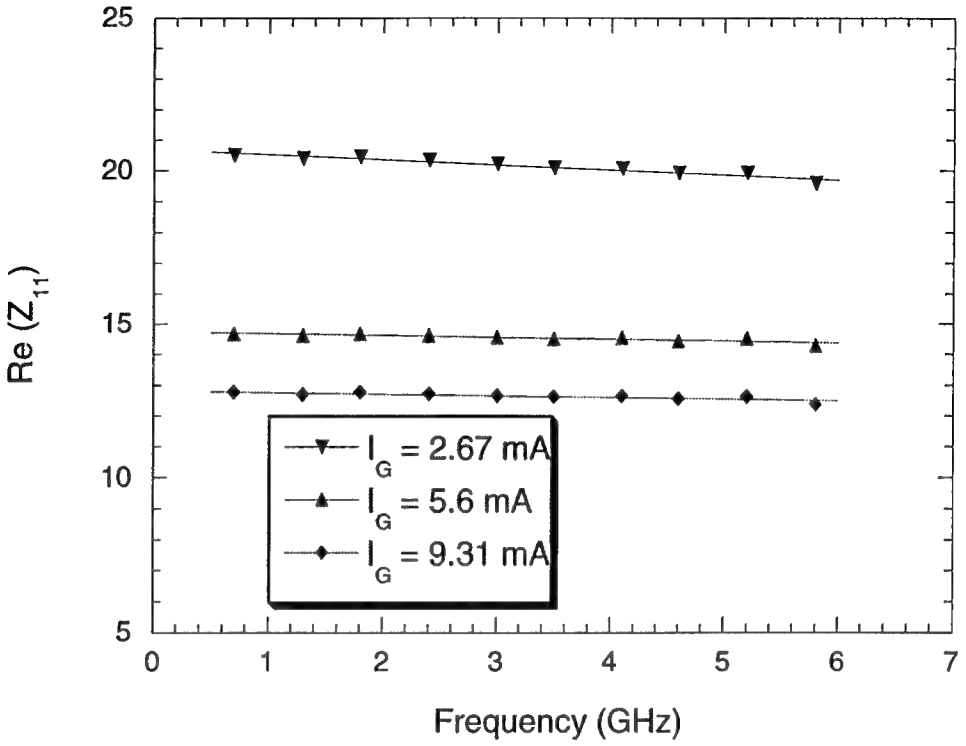

Fig. 14a

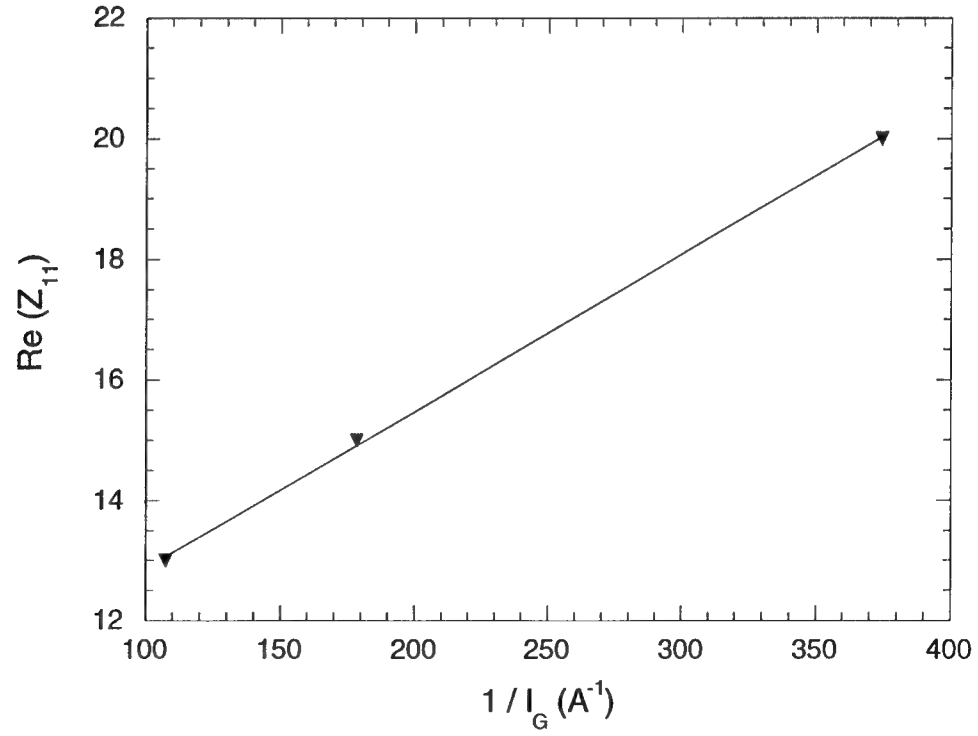

Fig. 14b

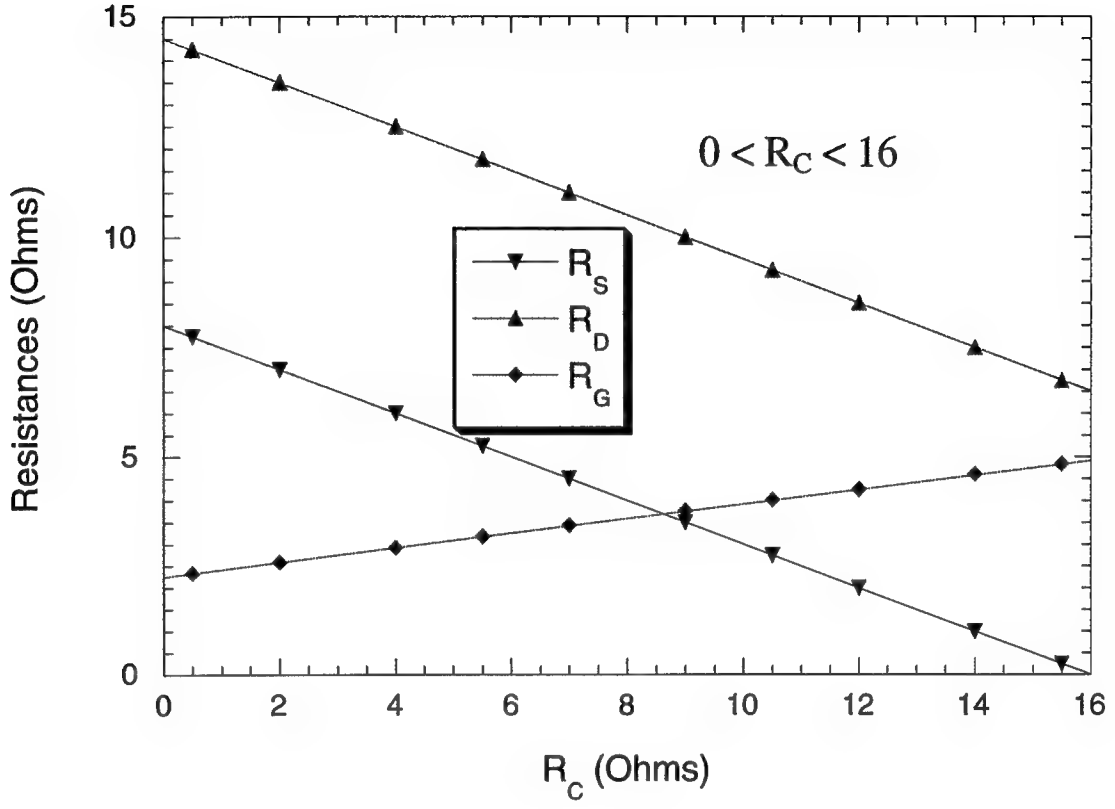
15
10
5
0
0
2
4
6
8
10
12
14
16
Resistances (Ohms)
R_C (Ohms)
$0 < R_C < 16$
R_S
R_D
R_G

Fig. 15

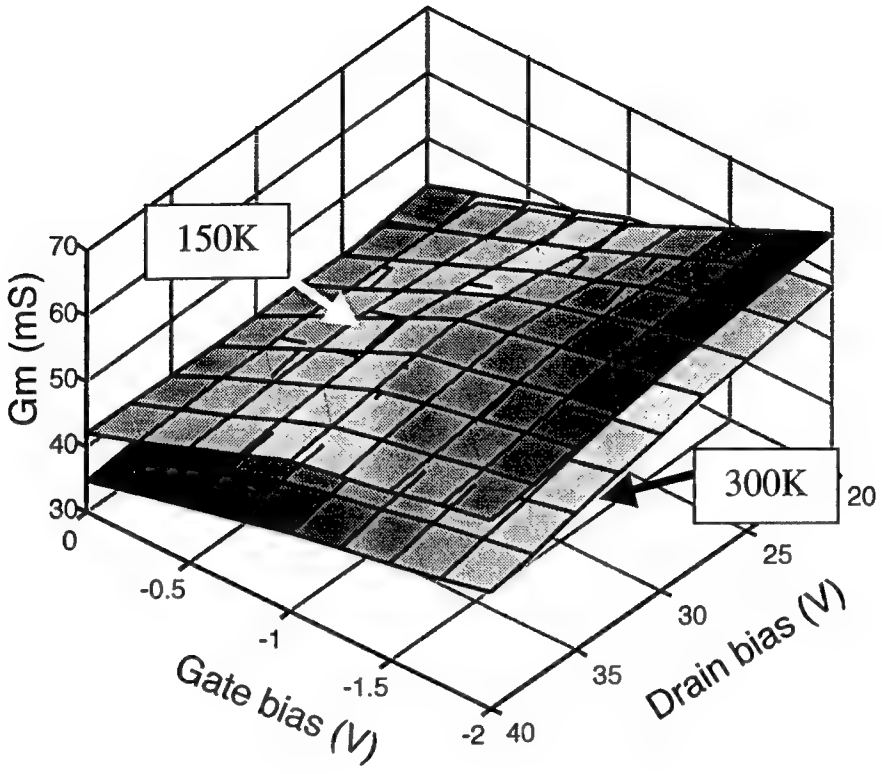

Fig. 16a

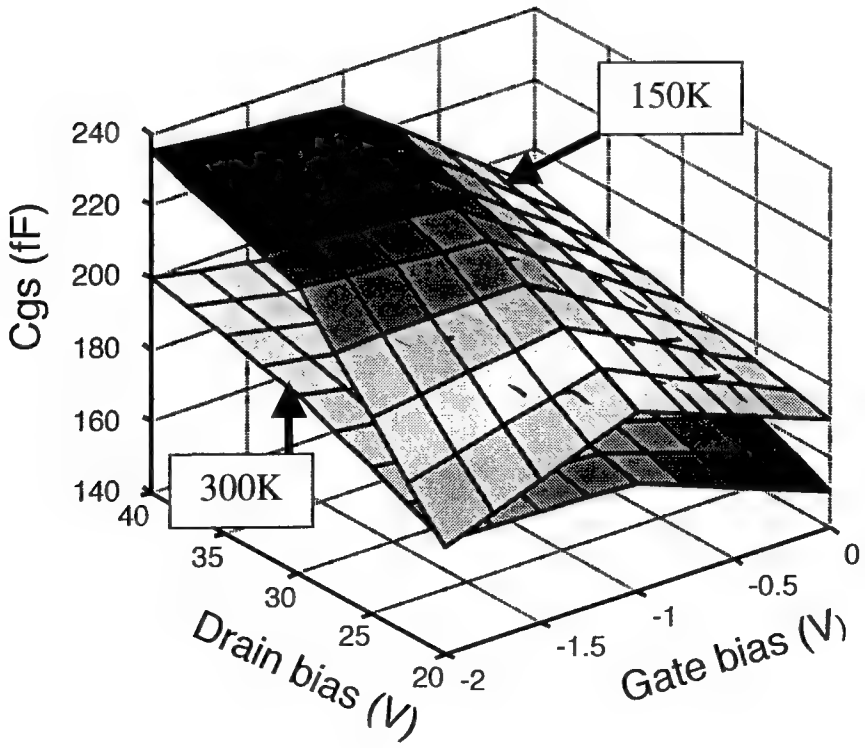

Fig. 16b

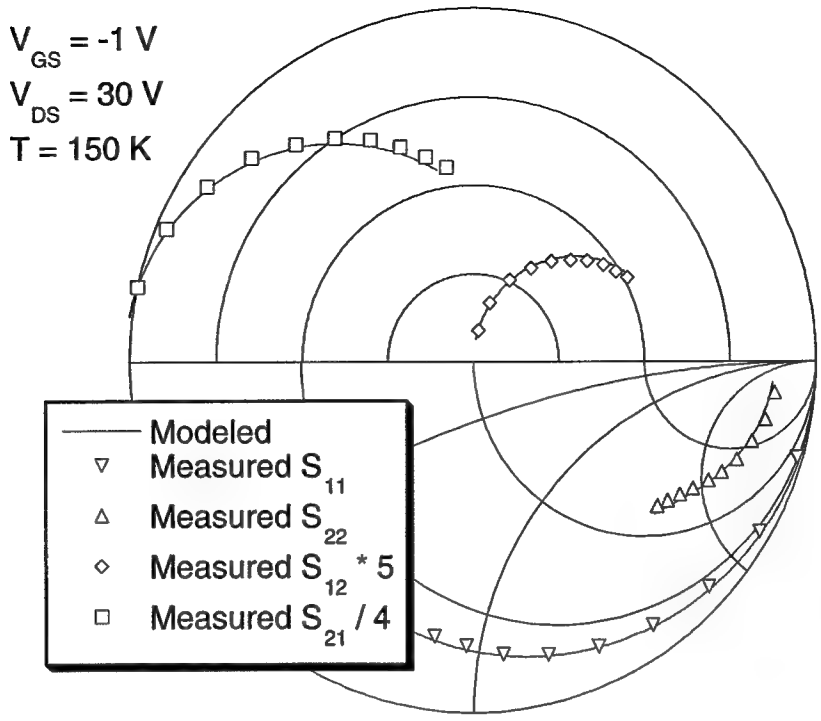

Fig. 17a

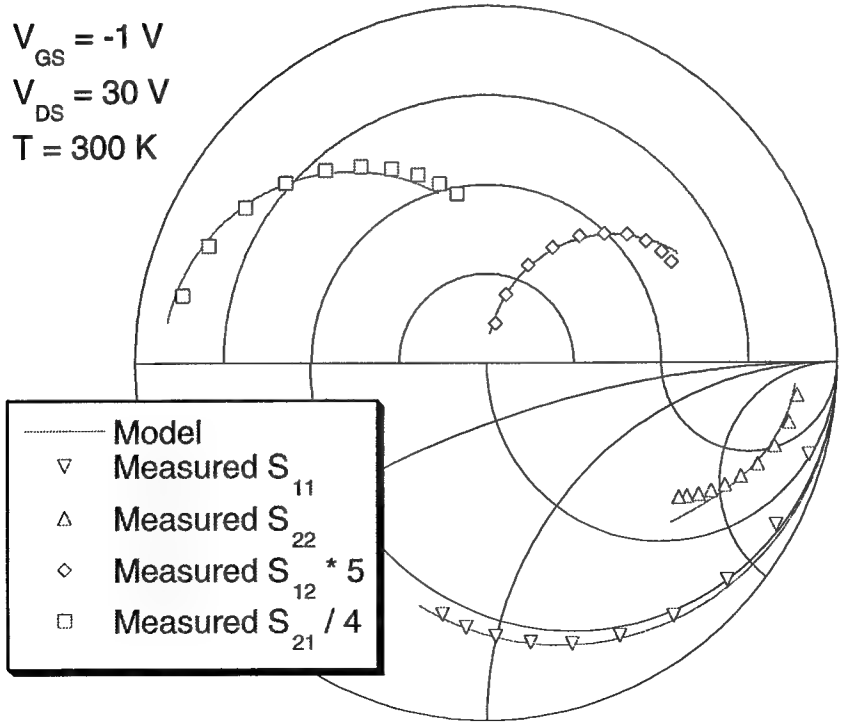

Fig. 17b

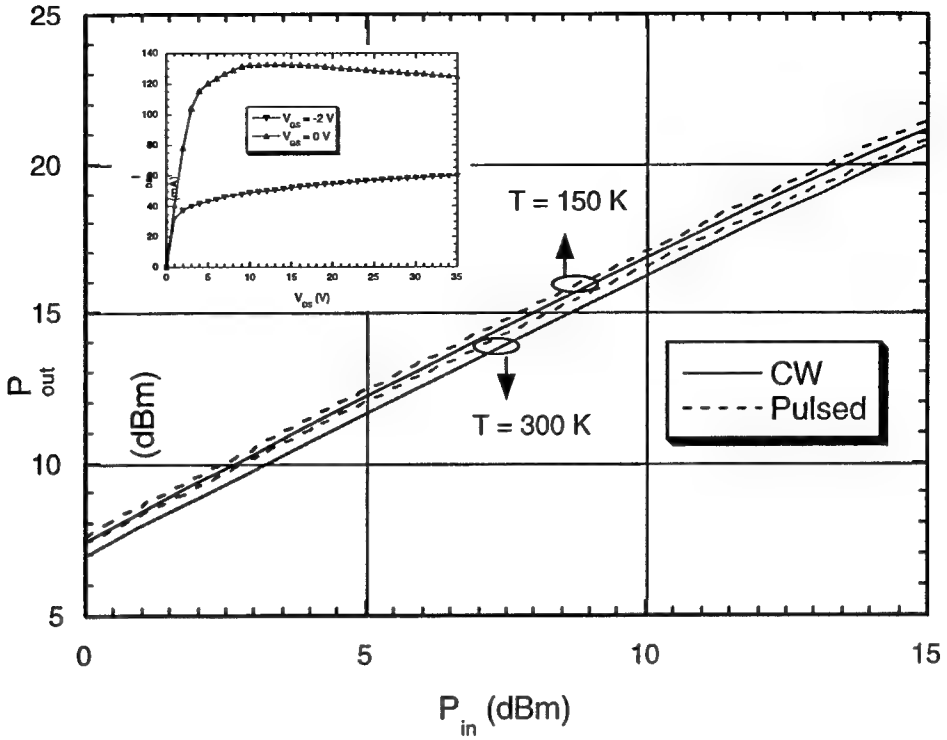
25
20
15
10
5
0
5
10
15
P out (dBm)
P in (dBm)
T = 150 K
T = 300 K
CW
Pulsed
V GS = -2 V
V GS = 0 V
V DS (V)

Fig. 18

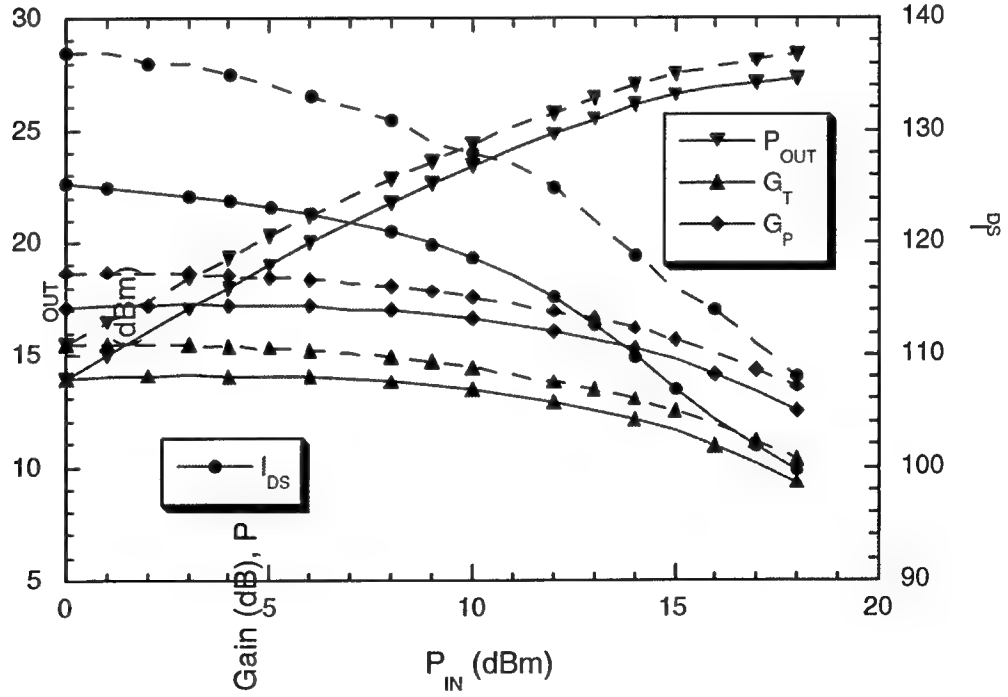
30
25
20
15
10
5
0
5
10
15
20
140
130
120
110
100
90
P OUT (dBm)
Gain (dB), P
P IN (dBm)
P OUT
G T
G P
I DS

Fig. 19

	C_{GS}	C_{DS}	C_{GD}	R_I	$1/G_{DS}$	G_M
T = 150K	210 fF	11 fF	21.5 fF	0.1 Ω	588 Ω	57 mS
T = 300K	182 fF	3.5 fF	26 fF	10 Ω	650 Ω	50 mS

Table 1

Study of Self-Heating Effects in GaN HEMTs

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***Abstract* — Pulsed RF and IV characterizations are performed on power GaN HEMTs. These measurements are carried out at different temperatures for the first time to understand self-heating effects and to investigate the possibility of improving heat dissipation mechanisms. These measurements are the basis for robust large-signal models.**

I. Introduction

The wireless communication market is growing rapidly and there is a great demand for high power transistors for applications such as phased array antennas and base stations. In these days, available power transistors are in the 1W/mm range. Candidates to fill the need for higher output power are Si-LDMOS, SiC and GaN based transistors. They offer power densities in the few W/mm range because of their high breakdown voltage [1-7]. GaN compared to SiC and Si-LDMOS, offers higher cut off frequencies and maximum frequencies of oscillation ($f_T \approx$ 25 GHz, and $f_{MAX} \approx$ 33 GHz) [2,4,5].

Studying devices under pulsed conditions and for different temperature of operation allows one to understand the thermal behavior and answer the question of whether or not improvements in heat sinks will ameliorate the device's characteristic. Additionally, studying devices under these condition enables one to build more robust large-signal models that help understand the device physics [6,8,9,10].

In this work we present fully characterized GaN HEMTs under pulsed conditions with the temperature as an additional parameter. Both IV and power RF characteristics are achieved in a continuous and pulsed mode up to 25 GHz and at temperatures down to 65 K.

II. Experimental Setup

The experimental setup consists of two pulse bias generators, a frequency source synchronized with the pulse generator enabling a pulse RF signal that is amplified to attain the required input power level at the DUT. The current is monitored with a digitizing scope through a current probe. The RF power is monitored with a peak power meter. Measurements are achieved at a gate baseline that is in the pinch-off region of the DUT. Both the drain and RF pulse width are shorter and delayed by few 100ns in order to center them in the gate pulse. Fig. 1 presents a diagram of the setup used.

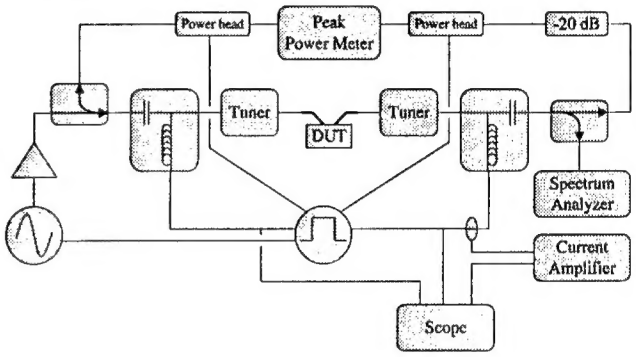

Fig. 1 Schematic of the measurement system.

Measurements have been carried out on AlGaN/GaN HEMTs from 300K to 65 K using a cryogenic probe station [4,9]. The samples are provided by CREE Inc. and are grown on a SiC substrate, with a gate width of 125 µm per finger. Measurements were performed on different devices with various gate lengths and number of fingers. In this work we present the results of a 2-finger device with a gate length L_G = 0.35 µm, a gate to source L_{GS} = 0.1 µm, and gate to drain L_{GD} = 3 µm.

III. Influence On Large Signal Modeling

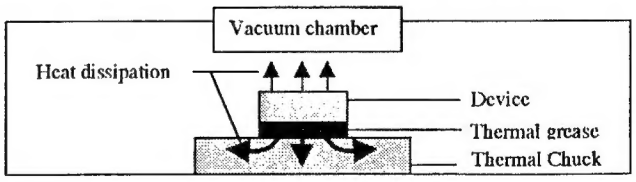

Fig. 2. Heat dissipation and thermal path for measurements.

The discrete device is mounted in a high vacuum cryogenic chamber cooled by a closed cycle helium refrigerator, as shown in Fig. 2. To insure good heat dissipation from the device to the cold head a perfect contact needs to be guaranteed. This is achieved with a thermal grease compound. Studying devices under these

conditions allow us to understand the transistor's junction temperature under pulsed and continuous mode of operation and enable us to accurately build a robust model that include those parameters. In Fig. 3 we show the large-signal model extraction procedures [6].

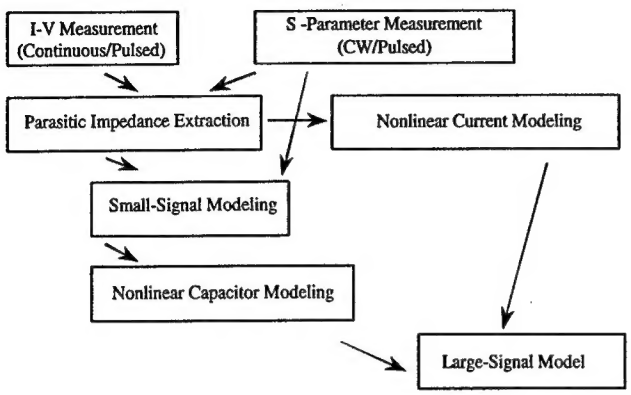

Fig. 3. Large-signal modeling flow diagram.

IV. Results

The GaN HEMT DC characteristics show an increase in the drain current and the device transconductance while operating at reduced temperature (Fig. 4). The improvements are results of an increase in electron mobility [12].

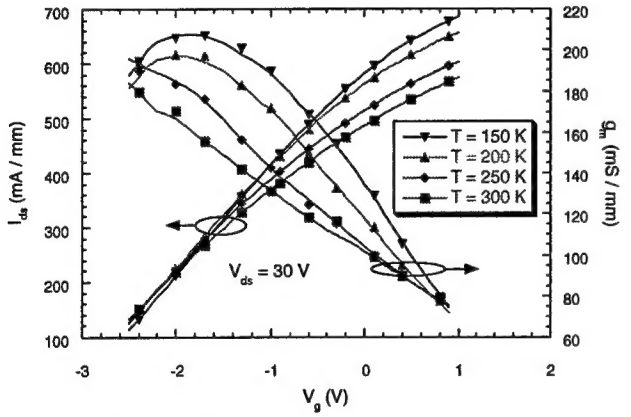

Fig. 4 Transconductance and drain current versus V_{GS} for various temperatures at V_{DS} = 30 V.

Fig. 5 exhibits pulsed-IV measurement characteristics at 300 K for various duty-cycle at 0 V gate bias and a pulse period of 100 µs. By gradually reducing the pulse width the negative slope of the $I_{DS}(V_{DS})$ characteristics becomes less important.

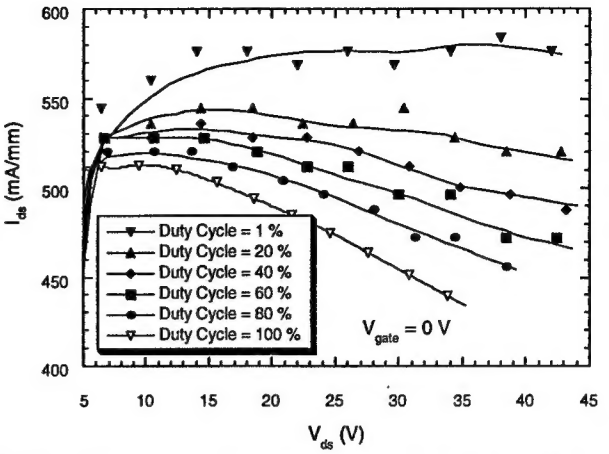

Fig. 5. Drain current for various duty cycles at V_{GS} = 0 V, at 300 K.

Fig. 6 compares the drain-to-source current at 300K and 65K under pulsed and continuous mode of operation. Pulsed characteristics are obtained with a signal period of 100 µs, and a pulse width of 1 µs on the drain side. Unlike at 300 K, pulsed and continuous I-V characteristics at T = 65 K correlate for drain voltages larger than 15 V. The mismatch observed at 65 K at low drain voltages has been reported in [13].

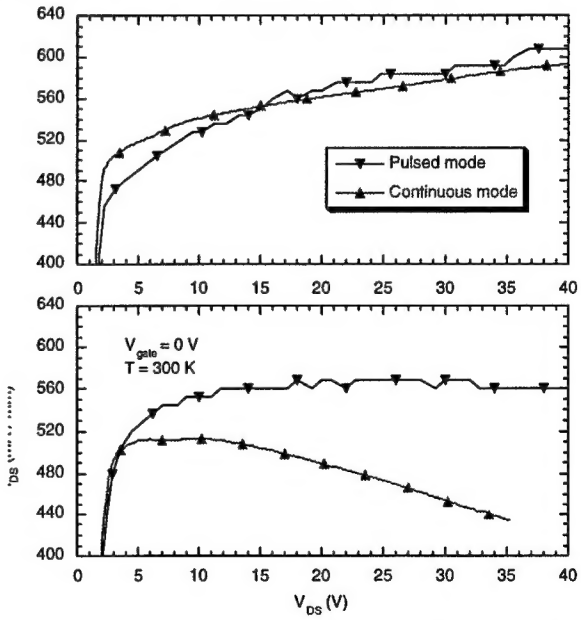

Fig. 6. Drain current at V_{GS} = 0 V under pulsed and continuous conditions at T = 65 K and T = 300 K.

Fig. 7 shows the temperature effects on DC-$I_{DS}(V_{DS})$ and DC-$I_{GS}(V_{DS})$ characteristics. At any temperature, it is possible to define the drain voltage threshold as the drain voltage value at which the drain current starts to decrease. It is noteworthy that as the temperature decreases, the

drain voltage threshold increases. This is interpreted as an extension of the drain voltage range for which the DUT does not suffer from self-heating. At the same time a decrease in the temperature reduces the gate current.

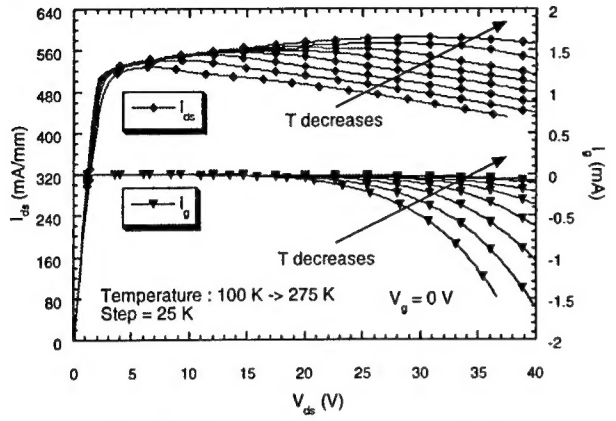

Fig. 7. Drain and gate current for various temperatures at V_{GS} = 0 V.

At any bias and temperature conditions it is possible to define the pulse width threshold as the pulse width that leads to a drain current saturation. Fig. 8 displays the pulse width threshold for V_{DS} = 45 V, V_{GS} = 0 V, a period of 100 µs, and at several temperatures. We observe that at 150 K, the drain current is saturated at all available pulse widths. This is perceived as an absence of any heating effects. Above 225 K the drain current could not be saturated at any available duty-cycle (the minimum duty-cycle used was 1 %). Therefore, it is possible to say that the pulse width threshold is below 1 µs for temperatures greater than 225 K. For temperatures between 150 K and 225 K saturation of the drain current was observed, and thus a threshold value was extracted. We observed that the threshold value to achieve drain current saturation increases while temperature decreases, meaning that a reduction in the external temperature decreases self-heating effects in the device. Fig. 8 also shows the pulse width threshold as a function of temperature for two different bias conditions.

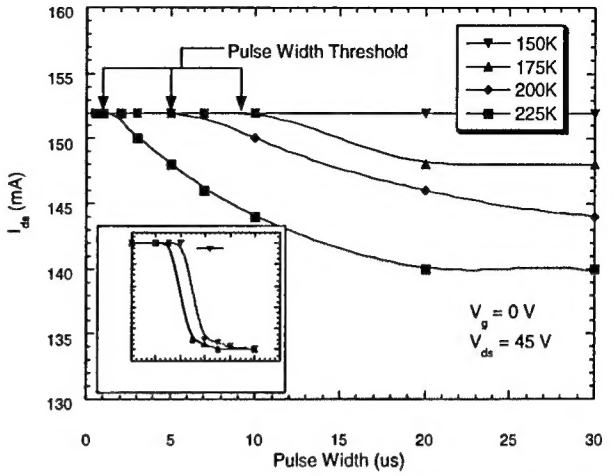

Fig. 8. Drain current versus pulse width for pulse width threshold determination (isothermal environment) at various temperatures.

Fig. 9 shows the short-circuit current gain and the maximum available gain under different temperature conditions. The cutoff frequency (f_T) and the maximum frequency of oscillation (f_{MAX}) improve while reducing the temperature of operation.

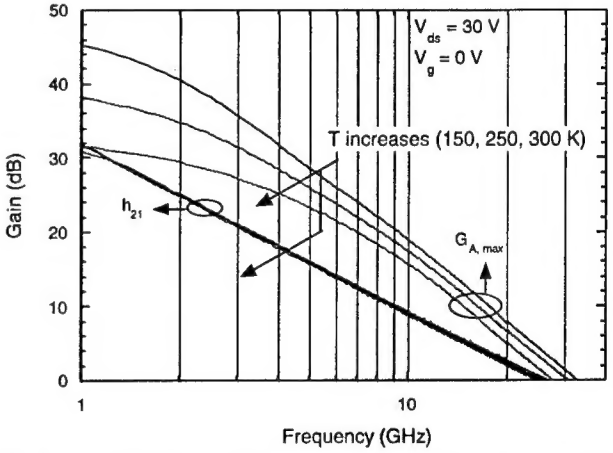

Fig. 9. Short circuit current gain and maximum available gain at different temperatures (300, 250, 150 K)

Finally, Fig. 10 shows the RF power performance of the GaN HEMT sample when operated at reduced lattice temperature. Measurements are achieved under pulsed and CW mode of operation. As the temperature decreases the heating effects become less important resulting in little difference between CW and pulsed RF/bias power measurements. The pulsed power measurements are achieved with a 5µs pulse width on the gate side, a 3µs pulse width for the drain, and a 2µs pulse width for the RF signal.

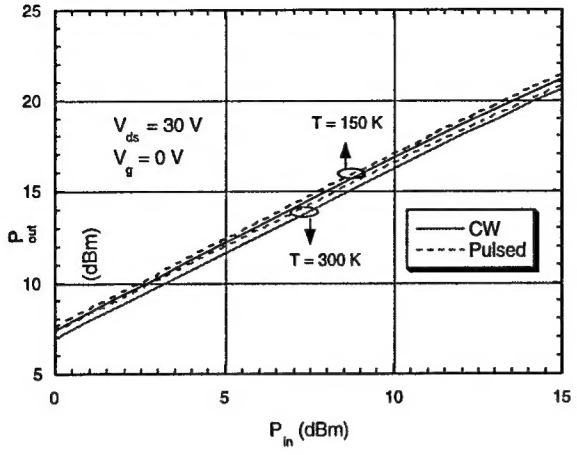

Fig. 10. Output power versus frequency under pulsed and continuous conditions into 50 Ohms termination at T = 150 K and T = 300 K (V_{DS} = 30 V, V_{GS} = 0 V).

V. Conclusion

Pulsed RF and I-V measurements are attained for the first time on GaN HEMT samples at different temperature conditions. The measurement results give an in depth understanding of the device behavior and are the basis for robust large-signal device modeling. Additionally, these measurements allow the understanding of the self-heating effects in GaN-based transistors and the possibility for device structure improvement resulting in better device performance.

Acknowledgement

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